Frequency Response Analyser SM 2001 & 2001S

Incorporating Reference Synchroniser SM2002

Instruction Manual

SIM2001

Digitized by the Internet Archive
in 2024

https://archive.org/details/manualsplus_03868

Instruction Manual

FREQUENCY RESPONSE ANALYSER

SM 2001

Issue 2

May 1973

© SE Laboratories (Engineering) Limited.

LIST OF AMENDMENTS

Al.No.	By Whom	Date
1	S.E. LABS.	April 1972.
2.	S.E. LABS.	Sept. 1972.
3.	S.E. LABS	MARCH 1973.

Al.No.	By Whom.	Date.

PREFACE

1. DAMAGE IN TRANSIT

1.1 Unpack the equipment and examine it thoroughly to ascertain whether any damage has occurred in transit. Report immediately any such damage to the agent or manufacturer. Retain the four rubberized packing surrounds, should a return to manufacturer be necessary.

2. GUARANTEE

2.1 All goods manufactured by the Company are guaranteed to the extent hereafter mentioned against defects arising from faulty material or workmanship subject to the goods not having suffered mal-treatment or interference. The Company's liability under this guarantee is limited to replacing any part or parts found defective within a period as laid down in Company instructions after the date of delivery or installation.

If goods not of the Company's manufacture are ordered, the guarantee of that company is to be accepted.

3. LOCAL AGENTS ADDRESS:-

3.1 The address of your local agent is:-

SERVICE DEPT. 01-750-5951

4. DESCRIPTIVE MATTER AND ILLUSTRATIONS.

4.1 Descriptive matter, illustrations, dimensions and weights issued by the Company are typical and shall not be held as binding. The Company reserves the right to alter patterns and designs without notice.

SAFETY MEASURES

1. This instruction manual contains certain

   — CAUTION — and — WARNING —

   notices which ***MUST*** be followed by the user to ensure ***SAFE*** operation and to retain the equipment in a ***SAFE*** condition.

2. All users of the equipment described in this manual ***MUST*** have received adequate training in its use and application in order to ensure ***SAFE AND PROPER USE***.

3. Any adjustment, maintenance and repair of the opened apparatus under voltage shall be carried out only by a skilled person who is ***AWARE OF THE HAZARD INVOLVED***.

AMENDMENT LIST NO.4
TO
FREQUENCY RESPONSE ANALYSER SM 2001
ISSUE 2, MAY 1973

1. PURPOSE

This amendment brings up to date the 'equipment check list' in Section 3 (page 3.1),contains a modification to the harmonic selection check given in Section 5 (page 5.2) and gives details of circuit diagram changes.

2. HAND AMENDMENTS

SECTION	PAGE	PARA	LINE	CHANGE
3	3.1	3(b)and (c)	2 and 3	...Delete all reference to McMurdo 50-way plug and socket,and accessories.
3	3.1	3	-	...Add the following note to end of Para: 'Mating connectors for the SM 2001 rear panel sockets are not supplied with the SM 2001 instrument,but an interconnecing cable,complete with connectors is supplied with the SM 2003,SM 2004,SM 2007 and SM 250 complementary units'.

3. NEW PAGES

Section 2,Pages 2-1,2-2. ...Fig.2-1 now shows instrument with modified displays and additional AUTO control.

Section 3,Pages 3-3,3-4. ...Fig.3-1 now shows the operator section with modified generator display window.

Section 3,Pages 3-5,3-6. ...Fig.3-2 now shows the correlator section with additional AUTO control.

Section 3,Pages 3-9,3-10. ...Fig.3-3 now shows modified positions of rear panel connectors.

Section 5,Pages 5-1,5-2. ...New page 5-2 contains changes to the table in Para.3.3(b).

Section 6. ...Add to the end of this section,the new diagrams entitled:

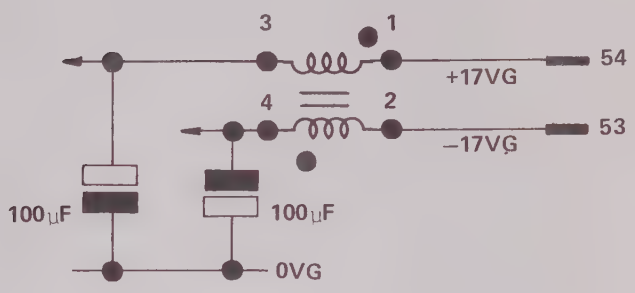
General Block Diagram (SM2001A) E41669
Power Supply SE3A (SM2001A) - Circuit Diagram

Add these titles to the end of the 'List of Contents',referring to Section 6

4. CIRCUIT DIAGRAM CHANGES (SECTION 6)

Board B,Dwg.No. E32670

...Add a toriod filter to the $\pm 17V_G$ input pins 53 and 54 as shown below:



Board C,Dwg.No. B32671

...Add component references to the following counter IC's:

(i) Label the IC,SN74191N,pin 4 connected to gate IC5 as IC6.

(ii) Label the IC,SN74191N,pin 4 connected to gate IC5,pin 12 as IC12.

(iii) Label the IC,SN74191N,pin 4, connected to gate IC2,pin 6 as IC9.

(iv) Label the IC,SN74191N,pin 4 connected to gate IC2,pin 12 as IC14.

Replace the origin of the clock input to bistables IC4 and IC13 from gate IC1/10 to come from IC1/12.

Connect a 1k resistor,R31 from board pin 46 (sync I/P) to the $+5V_E$ supply.

Board E,Dwg.No. E32673

...Connect a 10,000pF capacitor from IC2, pin 9 to $0V_E$, ref C33.

Label board pin 44a as 0V
Label board pin 45a as 0V
Label board pin 46a as +5V
Label board pin 47a as Data A I/P.

Board F,Dwg.No. E32674

...Connect a 2.2k resistor between gate IC40,pin 13 and $+5V_E$.

Re-annotate R7 as R3
Re-annotate R8 as R4

SM2001/AL4

Board G,Dwg.No. B32684

...Connect a 2.2k resistor between board pin 4 (reset) and $+5V_E$

Connect a 2.2k resistor between board pin 3 ($\overline{IT}$) and $+5V_E$

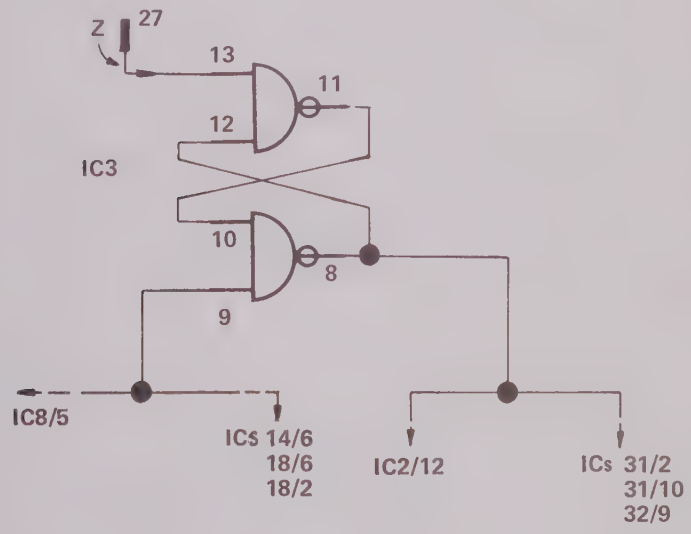
Board K,Dwg.No.E32746

...Re-annotate the input pins to gates IC31/8 & IC32/8 as follows:

Old pin No.		New pin No.
IC31/11	becomes	IC31/10
IC31/10	becomes	IC31/11
IC32/10	becomes	IC32/9
IC32/9	becomes	IC32/10

Break the link between bistable IC18, pin 10 and gates IC2/12,IC31/2,IC31/10 and IC32/9 (as changed in previous para).

Add the circuit shown below in place of the link broken at bistable IC18,pin 10 above.



Connect R16,2.2k,between board pin 17 and $+5V_E$
Connect R17,2.2k,between board pin 22 and $+5V_E$

Disconnect C27 from the junction of R7 and TR3 base.
Connect C27 to TR3 collector.

Board L,Dwg.No. B32745

...Connect R3,2.2k between bd. pin 16 & $+5V_E$
Connect R4,2.2k between bd. pin 15 & $+5V_E$
Connect R5,2.2k between bd. pin 22 & $+5V_E$
Connect R6,2.2k between bd. pin 21 & $+5V_E$

SM2001/AL4

Board N,Dwg.No. 32676

...Change board pin 1 to pin 2 (ϕ control)
Change board pin 2 to pin 1 (Log control)

Change Function 'F.H.' to
'F.H.,board pin 4'.
Change Function 'F.H.' to
'F.H.,board pin 3'.

Board P,Dwg.No. E32743

...Re-annotate board pins 33,35,37 and 38 as follows:

Pin 33 should read 'Sin Product/N'
Pin 35 should read 'Cos Product/N'
Pin 37 should read 'I/P Cos Clock'
Pin 38 should read 'I/P Sin Clock'

Insert a resistor,100 ohms,in series between gates IC8/1 and IC7/9. Add a capacitor,2,700p between IC7/9 and $0V_E$.

Display Board,Dwg.No.E32699

...Add the following note to the diagram:

'To identify the input pin nos.of the Frequency & Voltage Display Board,Cosine Register Display Board and Sine Register Display Board,refer to the Earthing Section Interconnection Block Diagram E32689'.

Board S,Dwg.No. B32744

...Connect a line,terminated by board pin 7,to pin 5 of gate IC21/6. Label pin 7 as 'Reset to 8-bit BRM'.

Break the connection between IC1/10 and IC1/1,*leaving the other lines connected*. Connect the input to IC1/1 to IC1/5.

Re-annotate the function on board pin 27 as 'UP SIN'.
Re-annotate the function on board pin 28 as 'DOWN SIN'.
Re-annotate the function on board pin 12 as 'I/P COS PRODUCT'.
Re-annotate the function on board pin 24 as 'O/P COS PRODUCT'.
Re-annotate the function on board pin 22 as 'I/P SIN PRODUCT'.
Re-annotate the function on board pin 23 as 'O/P SIN PRODUCT'.

Label the Clock $\propto$ NF2 input pin as 'pin 11'.

Board S,Dwg.No. B32744 (cont)

...Bistable IC27/13 wrongly labelled.

Pin 13 should read pin 8.
Pin 12 should read pin 9.
Pin 14 should read pin 7.
Pin 1 should read pin 5.
Pin 3 should read pin 10.

Circuit block IC1/12 (connected to board input pin 10 'SYNC') should read IC1/8.

Board T.Dwg.No. B32678

...Add note 3 as follows:

'Select TR5,7,9,11,13,15,17,19 and 21 using SE Spec No.TSP160'.

Add to C1, '16V'.

Board U.Dwg.No. B32679

...Change transistors TR4 to TR11 to type BC182L.
Transistors TR15 & TR17 are type BFY51.
Add a test point,TP4,at the output of IC8/6.
Add to the transistor test spec.note in the notes column,the test-spec.number C40665.

Board V.Dwg.No. B32680

...Change the value of C1 to 100 µF.
Connect a series network R37,2,7k and C21,150pF,between the junction of OA1, pin 1 and relay contacts RL6/RL7,and the 'Lo' line (Board pin 5) such that C21 connects to the 'Lo' line.

Earthy Section Interconnection Block Diagram E32689

...On the Display Switches (C,P,P/dB)connect the three vacant pins together to $+5V_E$.

On the Cycles of Integration Control PCB (K): Add board pins 27 and 7.

Connect board pin 27 (above) to board pin 2 on the Polar Log Control PCB (P).

Connect board pin 7 (above) to board pin 7 on the Polar Log Control PCB (P).

On the Sin Register PCB (N) re-label the following board pins:

Old Nos.		New Nos.
Pin 1	becomes	Pin 2
Pin 2	becomes	Pin 1
Pin 5	becomes	Pin 4
Pin 4	becomes	Pin 3

---

5. ADDITIONAL OPERATING NOTES.

Section 3, Page 3-8. Add between para 7.1.1 and 7.1.2 the following caution:
'The SM2001 does not function correctly if leads are plugged into the rear panel connectors unless these leads are connected to the ancillary equipment (e.g. SM2003) AND THE ANCILLARY EQUIPMENT IS SWITCHED ON.'

SM2001/AL4

Section 3, Page 3-6, Para 6.2,(c)

Absolute Ranges

The first line of the "Note" should read:

' 50 % (approx) overrange is provided'

SECTION 5

MAINTENANCE

1. INTRODUCTION

1.1. This section contains notes on preventive maintenance, an in-cabinet functional check and internal adjustment procedures.

2. PREVENTIVE MAINTENANCE

2.1. Instrument Cover Removal

2.1.1. To remove the top cover, loosen and remove the six cover retaining screws from the top of the instrument.

WARNING

115V or 230V a.c. and d.c. supply wires are exposed when the cover is removed.

2.2. Cleaning

2.2.1 The instrument should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation.

2.2.2. Thoroughly clean both the inside and outside of the instrument. Remove dust from inaccessible areas with low pressure compressed air or vacuum cleaner. Use alcohol applied with a cleaning brush to remove accumulations of dirt or grease from connector contacts and component terminals. Clean the exterior of the instrument and the front panel with a mild detergent mixed with water, applying the solution with a soft, lint-free cloth.

2.3. Visual Inspection

2.3.1. The instrument should be inspected occasionally for such defects as broken connections, loose, broken or frayed wiring, dirty or pitted switch and connector contacts and cracked or broken printed circuit boards. Often, before a total or partial failure occurs, a deteriorating component can be located due to obvious discoloration, cracking or warping. Care must be taken if heat-damaged parts are located. Over-heating is usually only a sympton of trouble. For this reason, it is essential to determine the actual cause of over-heating before the heat-damaged part is renewed, otherwise, the damage may be repeated.

2.4. Repair and Renewal of Parts

2.4.1. Repair and replacement of electrical and mechanical parts must be accomplished with caution. Printed circuit component boards can become warped, cracked or burnt from excessive heat or mechanical stress. The following repair techniques are suggested to avoid inadvertant destruction or degradation of parts and assemblies.

2.4.2 Use ordinary 60/40 solder and a 35 to 40-watt pencil type soldering iron on the circuit board. The tip of the iron should be clean and properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the circuit from the base material. To desolder components use a commercial "solder sipper".

Always replace a component with its exact duplicate as specified in the parts list.

3. IN-CABINET CHECKS

3.1. The procedure outlined in the following paragraphs can be used to verify the operation of the SM2001. It can be used:

(a) as part of the incoming inspection check,
(b) periodically, for instruments used in systems,
(c) after repairs or adjustments, before returning the instrument to regular service

For the following checks, it is not necessary to remove the top cover.

3.2. Cycles of Integration Check

(a) Connect the GENERATOR OUTPUT terminals to the CORRELATOR INPUT terminals (HIGH to HIGH, LOW to LOW).

(b) Set the front panel controls to the positions listed in the table below and check that the time taken for a display to appear is always 1 second.

Generator Voltage	Generator Frequency (Hz)	Cycles of Integration	Display Reading	Display Time Delay (seconds)
9.99V	1	1	9.99	1
9.99V	10	10	9.99	1
9.99V	100	100	9.99	1
9.99V	999	1000	9.99	1

(c) Check that the centre display reads correctly as shown.

3.3. Harmonic Selection Check

(a) Set the generator frequency to 9.99Hz. Set the generator output voltage to 9.99V. Select 10 cycles of integration. Set the MEASUREMENT selector to the ABSOLUTE IV range. The OVERLOAD indicator should light-up; for the purposes of this test it can be ignored.

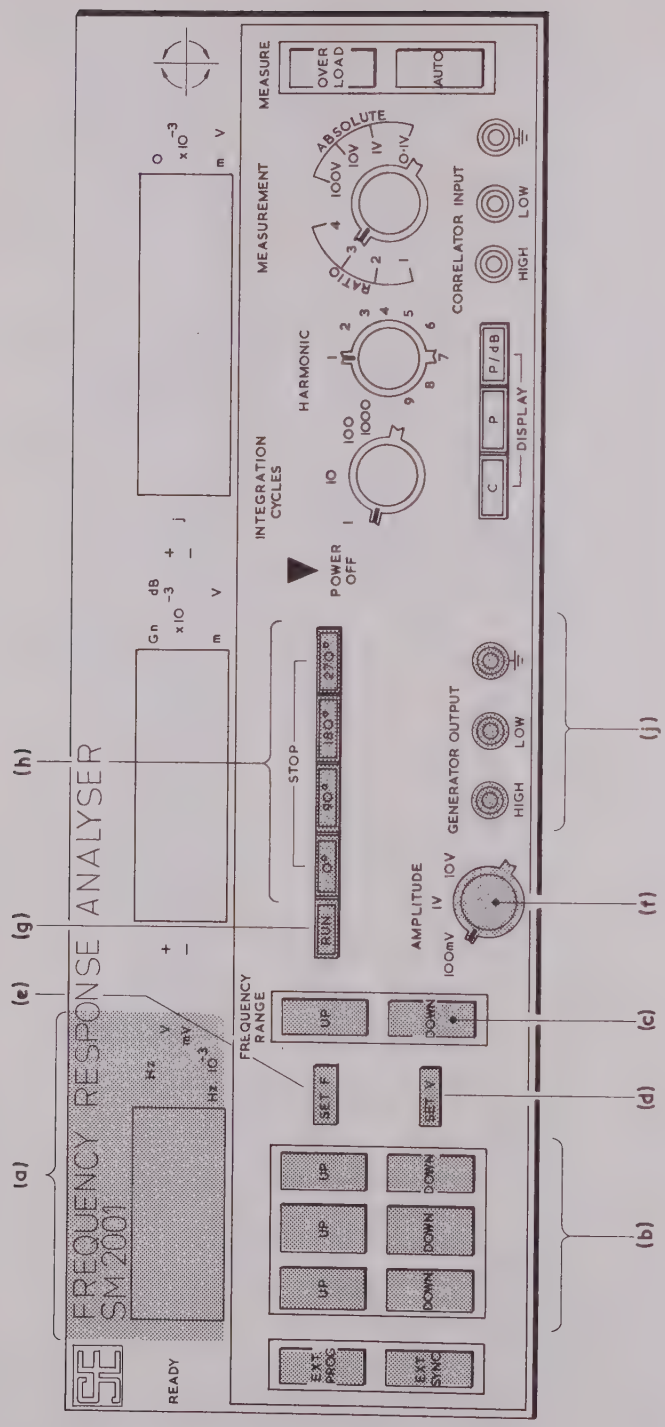
(b) Check the displayed results against the following table in relation to the position of the HARMONIC selector. To obtain a new reading at each position, the MEASURE push-button must be depressed.

HARMONIC Selector Posn.	Centre Display (V)	R.H. Display (V)
1	+0.280	−0.596
2	0.000	0.000
3	+0.655	−0.004
4	0.000	0.000
5	+0.363	−0.003
6	0.000	0.000
7	+0.230	−0.003
8	0.000	0.000
9	+0.150	−0.003

(c) Disconnect the generator output from the correlator input.

NOTE: This is an operational test only and all readings are very approximate.

Manual Change SM2001/AL4



(a) GENERATOR DISPLAY

(b) GENERATOR OUTPUT PUSH-BUTTONS

(c) FREQUENCY RANGE PUSH-BUTTONS

(d) SELECT FREQUENCY (SET F) PUSH-BUTTON

(e) SELECT VOLTAGE (SET V) PUSH-BUTTON

(f) AMPLITUDE (RANGE) SELECTOR

(g) RUN PUSH-BUTTON

(h) QUADRANT PUSH-BUTTONS

(j) GENERATOR OUTPUT TERMINALS

MANUAL CHANGE SM2001/AL4

FIG.3-1 GENERATOR SECTION-CONTROLS AND INDICATORS

waveform to stop when it reaches the quadrant point engraved on the button.

(j) GENERATOR OUTPUT terminals

The HIGH and LOW terminals are fully floating, greater than 100 MΩ to ground. The earth terminal is connected to chassis (line ground).

6.2 Correlator Section (Fig. 3.2)

(a) CORRELATOR INPUT Terminals

The signal to be measured is connected to the HIGH and LOW terminals. The input is fully floating, isolation >100MΩ to ground. Input impedance 1MΩ on all ranges. The earth terminal is connected to chassis (line ground).

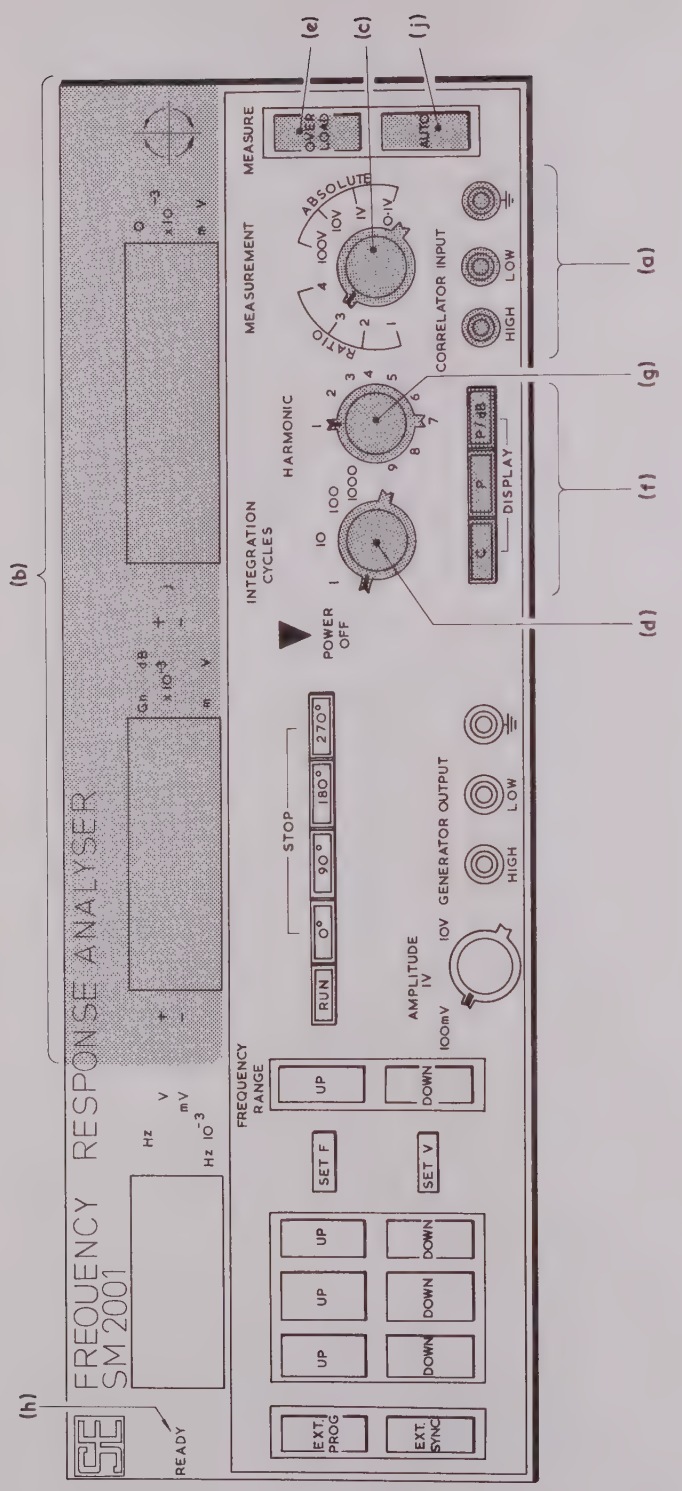
(b) Correlator Displays

(i) Cartesian Display
Two 4-digit displays using side-view numerical indicator tubes. Full scale of 1000 with overrange to 1500. Both displays have polarity indication and switched decimal points. Units are V and mV (in absolute mode) and no units or $x10^{-3}$ (in Ratio mode).

(ii) Polar Display
In this display mode, the centre display indicates the modulus of the input voltage or ratio, and the R.H. display indicates phase angle (to 0.1 degree resolution). Maximum phase angle indication is 90 degrees and the quadrant display indicates the reference axes.

(iii) Log Polar Display
In this display mode, the phase angle is displayed on the R.H. display. The centre display indicates the modulus in decibels, relative to Generator Section output (in ratio mode) or relative to 10V peak (in absolute mode).

(iv) Quadrant Display
Located immediately to the right of the R.H. display, phase angle quadrants 1 to 4 are indicated in the Polar and Log Polar modes, moving in anti-clockwise direction.



(a) CORRELATOR INPUT TERMINALS

(b) CORRELATOR DISPLAY

(c) MEASUREMENT SELECTOR

(d) POWER AND INTEGRATOR CYCLES SELECTOR

(e) MEASURE PUSH-BUTTON/OVERLOAD LAMP

(f) DISPLAY PUSH-BUTTONS

(g) HARMONIC SELECTOR

(h) READY INDICATOR

(j) AUTO PUSH-BUTTON

MANUAL CHANGE SM2001/AL4

FIG. 3-2 CORRELATOR SECTION - CONTROLS AND INDICATORS

(c) MEASUREMENT Selector:

8-position rotary switch, having 4 RATIO ranges and 4 ABSOLUTE ranges. This selector adjusts the sensitivity of the correlator to suit the amplitude of the input signal. It should be set to provide the greatest resolution of display.

Ratio Ranges

4 Ratio ranges are provided for use where gain measurements are required, the reading being in terms of gain:

Range 1: Full scale for an input of 0.01 times the Generator's AMPLITUDE setting on 10V range

Range 2: Full scale for an input of 0.1 times the Generator's AMPLITUDE setting on 10V range

Range 3: Full scale for an input of 1 times the Generator's AMPLITUDE setting on 10V range

Range 4: Full scale for an input of 10 times the Generator's AMPLITUDE setting on 10V range

Note: No multiplication factors are required since the decimal points of the correlator's display are switched according to the Generator & Correlator range settings.

Absolute Ranges

100V Range: Up to full scale of 100V peak can be displayed.

10V Range: Up to full scale of 10V peak can be displayed.

1V Range: Up to full scale of 1V peak can be displayed.

0.1V Range: Up to full scale of 100mV peak can be displayed.

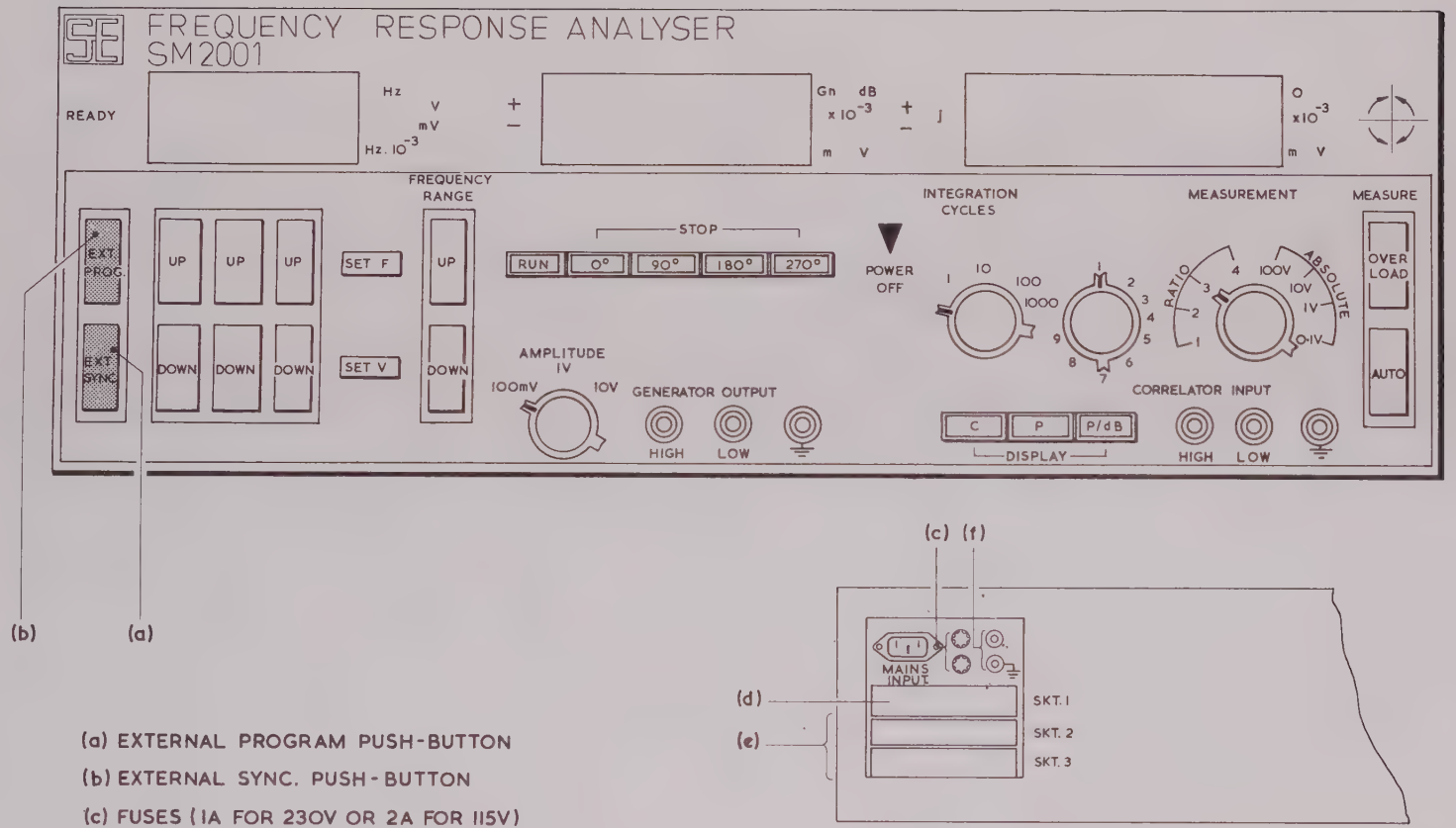
Note: 50% overrange is provided on all ranges of RATIO and ABSOLUTE measurements.

(d) POWER OFF/INTEGRATION CYCLES Selector:

5-position rotary switch with positions as follows:

POWER OFF to 1 : This switches on the instrument and at the same time selects 1 cycle of integration time of the correlator.

10, 100, 1000: Each numbered position denotes the number of cycles over which integration takes place.



REAR PANEL

(a) EXTERNAL PROGRAM PUSH-BUTTON

(b) EXTERNAL SYNC. PUSH-BUTTON

(c) FUSES (1A FOR 230V OR 2A FOR 115V)

(d) EXTERNAL PROGRAM (MALE) CONNECTOR SKT 1

(e) PRINTER OUTPUT (FEMALE) CONNECTORS SKT 2 & 3

(f) EXTERNAL SYNC. INPUT TERMINALS

FIG.3·3 EXTERNAL MODE FACILITIES

(f) Set the Generator Section output voltage amplitude to 9V as follows:

(i) Depress SET V.
(ii) Set AMPLITUDE TO 10V.
(iii) Operate each pair of the fine range UP:DOWN push - buttons until the generator display indicates 09.0V.

(g) Set the correlator MEASUREMENT selector to ABSOLUTE 10V, and HARMONIC selector to 1.

(h) Connect the output terminals of the generator section to the input of the correlator section (High to High, Low to Low).

(j) Depress the correlator DISPLAY C push-button.

(k) Set the INTEGRATION CYCLES selector to 10.

(m) Depress the RUN push-button.

(n) Allow a 5-minute warm-up time to elapse and then depress the MEASURE push-button. The following sequence should result:

(i) All displays cleared to zero and are extinguished (this occurs at the first quadrant point of the waveform).
(ii) READY indicator extinguished.
(iii) 0.5 second delay.
(iv) Displays present measurement reading. The centre display should read +09.00V $\pm$ 00.04V and the R.H. display should read 00.00, $\pm$ 00.03V.

(p) Depress the correlator DISPLAY P push-button. The centre display should read +09.00V, $\pm$ 00.04V. and the right hand display should read 000.0°, $\pm 000.3^{\circ}$. Quadrants 1 or 4 should be illuminated.

(q) Depress the correlator DISPLAY P/dB push-button. The R.H. display should read as in (p) above, and the centre display should read −001.0dB, $\pm$ 000.1dB. Depress the MEASURE push-button and check that the readings return to the same values.

7.2 Taking a Measurement

(a) Connect the input of the system-under-test to the Generator Section output terminals (HIGH and LOW) and connect the signal-to-be-measured to the Correlator Section (HIGH and LOW) terminals.

(b) Set the generator output frequency to the desired test frequency.

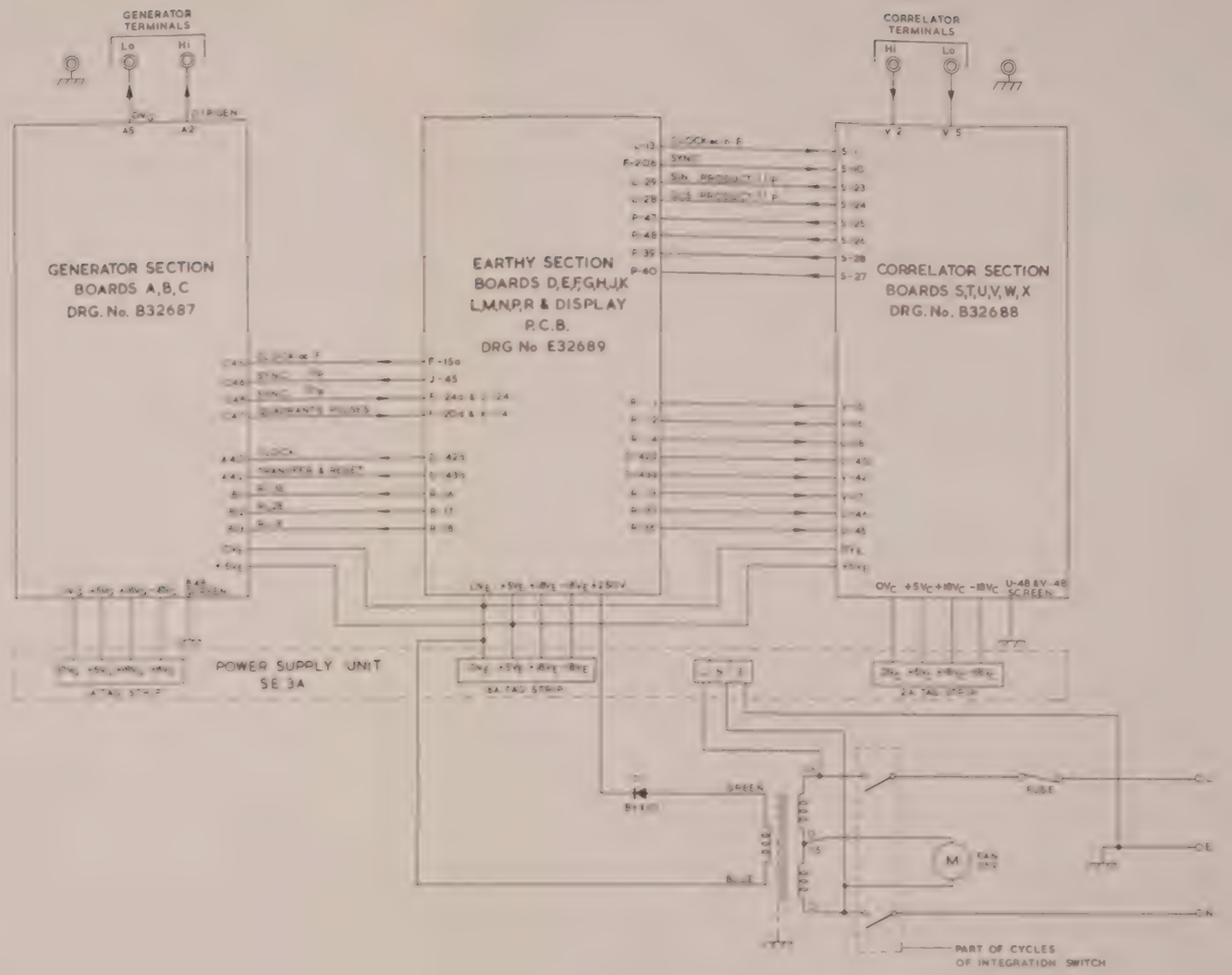
(c) Set the generator output voltage to the approximate desired test level.

(d) Set the number of cycles over which integration is to take place.

(e) Set the MEASUREMENT selector to the expected range (and mode required) of the signal-to-be-measured.

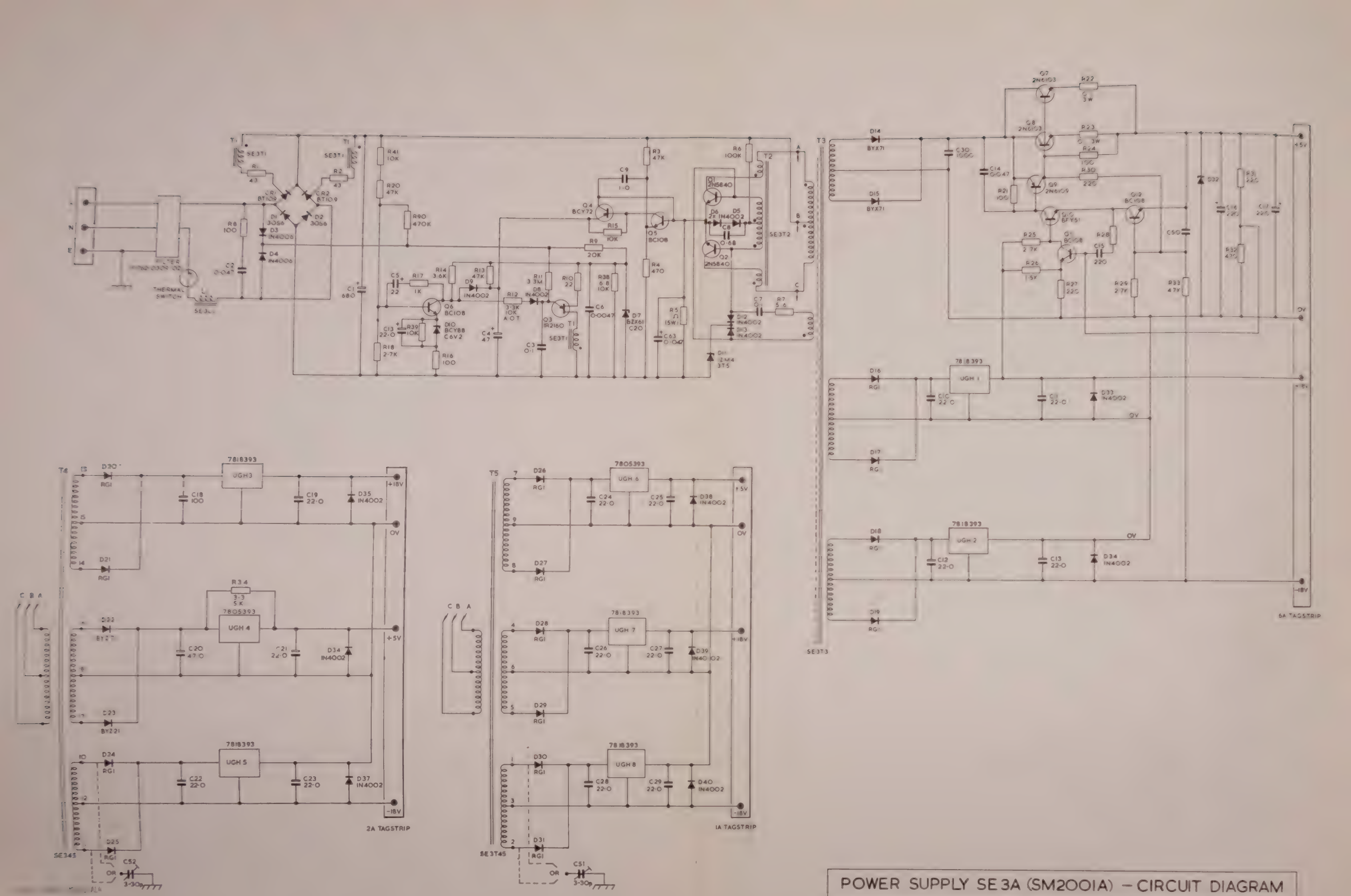
(f) Set the correlator displays to indicate cartesian, polar or polar dB as required.

(g) Depress the MEASURE push-button. After the measurement period has elapsed, the result is displayed. If the OVERLOAD indicator lights up during or after the measurement period, the measurement selector should be set to a higher range and the measuring sequence repeated. If the result is less than one tenth of full scale, the MEASUREMENT selector should be set to a lower range and the measuring sequence repeated.



P.C.B.	FUNCTION	CIRCUIT DIAG	PL No	P.C.B.	FUNCTION	CIRCUIT DIAG	PL No	P.C.B.	FUNCTION	CIRCUIT DIAG	PL No
A	VOLTAGE CONTROL GENERATOR	B32669	31495	K	CYCLES OF INTEGRATION CONTROL	E32746	30925	V	A/D CONVERTER	B32680	32540
B	D/A CONVERTER GENERATOR	E32670	31496	L	HARMONIC SELECTION CONTROL	B32745	30926	W	8 BIT BINARY RATE MULTIPLIER – COS	B32681	31488
C	DIGITAL OSCILLATOR GENERATOR	B32671	30920	M	COS REGISTER	B32675	30927	X	8 BIT BINARY RATE MULTIPLIER – SIN	B32691	31488
D	VOLTAGE CONTROL	B32672	30921	N	SIN REGISTER	B32676	30928		DISPLAY BOARD	E32699	30935
E	FREQUENCY CONTROL	E32673	30922	P	POLAR / LOG CONTROL	E32743	30929		FREQUENCY & VOLTAGE DISPLAY	"	30936
F	FREQUENCY RANGE CONTROL	E32674	30923	R	AMPLITUDE & CORRELATOR RANGE CONTROL	B32677	31486		COS REGISTER DISPLAY	"	30937
G	DECIMAL RATE MULTIPLIES & 6·74 MHz CLOCK	B32684	30924	S	DIGITAL OSCILLATOR CORRELATOR	B32744	30930		SIN REGISTER DISPLAY	"	30937
H	I/T GENERATOR ☐ (OPTION)	E32901	31496	T	D/A CONVERTER CORRELATOR	B32678	32539				
J	BALANCE CONTROL	B32902	31497	U	VOLTAGE CONTROL CORRELATOR	B32679	30933				

GENERAL BLOCK DIAGRAM (SM2001A) E 41669



POWER SUPPLY SE 3A (SM2001A) – CIRCUIT DIAGRAM

MANUAL CHANGE SM2001/AL5 MAY 1975

AMENDMENT LIST NO 5

TO

FREQUENCY RESPONSE ANALYSER SM 2001

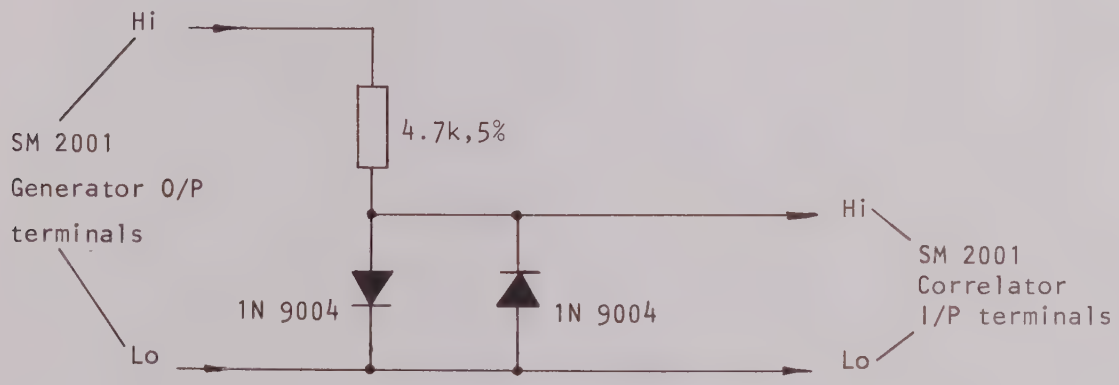
ISSUE 2, MAY 1973

1. PURPOSE

This amendment provides a more accurate harmonic selection check as given in Section 5 Maintenance,Para 3.3. The following procedure replaces that already in the manual. A minor change to circuit diagram B32669 is also included in this amendment.

2. HARMONIC SELECTION CHECK

(a) Make up the test network shown below and connect it to the SM 2001.



(b) Set the front panel controls as follows:

(i) Generator frequency to 99.9 Hz

(ii) Generator voltage to 9.99 V.

(iii) INTEGRATION CYCLES selector to 10.

(iv) Depress C (Cartesian) DISPLAY button.

(v) MEASUREMENT selector to 1 V ABSOLUTE.

HARMONIC Selector Posn.	Centre Display (V)	R.H.Display (V) ±5 bits
1	0.813, ± 10 bits	0.050
2	0.002, ± 5 bits	0.003
3	0.232, ± 5 bits	0.003
4	0.0019,± 5 bits	0.002
5	0.124, ± 5 bits	0.002
6	0.002, ± 5 bits	0.002
7	0.081, ± 5 bits	0.003
8	0.002, ± 5 bits	0.001
9	0.058, ± 5 bits	0.002

NOTE: The wide tolerances (especially on harmonic 1) are due to the temperature sensitivity of the diodes in the test network.

3. CIRCUIT DIAGRAM CHANGE

Board A,Dwg.No.B 32669 Change transistor TR19 to type BSX61

LIST OF CONTENTS

		Page No
Section 1	SPECIFICATIONS	1.1
	Frequency Response Analyser SM 2001	1.1
	Generator Section	1.1
	Correlator Section	1.2
	Operating Temperature Range	1.5
	Power Requirements	1.5
	Dimensions	1.5
	Optional Accessories	1.5
Section 2	GENERAL INFORMATION	2.1
	Introduction	2.1
	Optional Accessories	2.3
	Reference Synchroniser SM 2002	2.3
	Frequency Extension Unit SM 2003	2.3
	Modulator/Demodulator Unit SM 2004	2.3
	Theory of Operation	2.3
	Generator Section	2.4
	Correlator Section	2.7
Section 3	INSTALLATION AND OPERATION	3.1
	Introduction	3.1
	Unpacking	3.1
	Equipment Check List	3.1
	Rack Mounting	3.1
	Mains (Power Source) Checks	3.1
	Summary of Controls, Connectors and Indicators	3.2
	Generator Section	3.2
	Correlator Section	3.4
	External Mode Facilities	3.8
	Operating Instructions	3.8
	Initial Checks and Familiarisation	3.8
	Taking a Measurement	3.10
	Phase Angle Measurement	3.11
	Printer Output Facility	3.13
	External Programme Facility	3.15
Supplement No. 2002.	REFERENCE SYNCHRONISER SM 2002.	
	Specification	
	General Information	
	Installation	
	Operating Instructions	
	Application Notes	

SECTION 4

CIRCUIT DESCRIPTIONS

	Page No
Introduction	4.1
Generator Section	4.1
Voltage Control (Generator) Board A	4.1
Digital to Analogue Convertor (Generator) Board B	4.3
Digital Oscillator (Generator) Board C	4.4
Earthy Section	4.6
Voltage Control Board D	4.6
Frequency Control Board E	4.6
Frequency Range Control Board F	4.8
Crystal Oscillator and DRM Board G	4.10
System Description of Cartesian to Polar and Log Polar Conversion	4.10
Derivation of Cartesian Values	4.10
Conversion to Polar	4.12
Conversion to Log Polar	4.13
Cycles of Integration Board K	4.14
Harmonic Selection Board L	4.15
Cosine Register Board M and Sine Register Board N	4.16
Polar Log Control Board P	4.17
Amplitude and Correlator Range Control Board R	4.20
DisplayBoard	4.20
Correlator Section	4.21
Digital Oscillator (Correlator) Board S	4.21
Digital to Analogue Convertor (Correlator) Board T	4.21
Voltage Control (Correlator)Board U	4.22
Analogue to Digital Convertor Board V	4.24
Binary Rate Multiplier Boards W and X	4.25
Power Supply Unit	4.27
Mains Input (Link) Selection	4.27
Power Units Fitted to SM 2001,Suffix Nos /001 to /006	4.27
Power Units Fitted to SM 2001, Suffix Nos /007 to /025	4.28

SECTION 5

MAINTENANCE

Introduction	5.1
Preventive Maintenance	5.1
Instrument Cover Removal	5.1
Cleaning	5.1
Visual Inspection	5.1
Repair and Renewal of Parts	5.1
In-Cabinet Checks	5.2
Cycles of Integration Check	5.2
Harmonic Selection Check	5.2
Phase Checks	5.3
50 Hz Effect	5.3
Output Impedance Check	5.3
Internal Checks and Adjustments – SM 2001	5.4
Identification of PC Boards	5.4
Test Equipment Required	5.4
Power Supply	5.6
Generator Controls and Display Indicators Check	5.6
Crystal Oscillator Calibration (Board G)	5.8
Voltage Control (Generator) Board A– D/A Convertor Adjustment	5.8
Digital to Analogue Convertor(Generator) Board B	5.8
Voltage Control (Generator) Board C– Output Amplifier Adjustment	5.9
Digital Oscillator (Correlator) Board S	5.9

SECTION 5 (Cont'd)

	Page No.
Voltage Control (Correlator) Board U	5.10
Analogue to Digital Convertor (Correlator) Board V	5.10
Digital to Analogue Convertor (Correlator) Board T	5.11
Linearity Check	5.11
Internal Checks and Adjustments– SM 2002	5.11
Test Equipment Required	5.12
Input Amplifier and Balance Control Board J	5.12
1/t Generator Board H	5.12

SECTION 6 CIRCUITS AND COMPONENTS LAYOUT DIAGRAMS

Generator Section

Voltage Control (Generator) Board A	– Circuit Diagram B 32669 – Component Layout B 31480
Digital to Analogue Convertor (Generator) Board B	– Circuit Diagram E 32670 – Component Layout B 30706
Digital Oscillator (Generator) Board C	– Circuit Diagram B 32671 – Component Layout B 30920

Earthy Section

Voltage Control Board D	– Circuit Diagram B 32672 – Component Layout B 30921
Frequency Control Board E	– Circuit Diagram E 32673 – Component Layout B 30922
Frequency Range Control Board F	– Circuit Diagram E 32674 – Component Layout B 30923
Crystal Oscillator and DRM Board G	– Circuit Diagram B 32684 – Component Layout B 30924
Cycles of Integration Board K	– Circuit Diagram E 32746 – Component Layout B 30925
Harmonic Selection Board L	– Circuit Diagram B 32745 – Component Layout B 30926
Cosine Register Board M	– Circuit Diagram B 32675 – Component Layout B 30927
Sine Register Board N	– Circuit Diagram B 32676 – Component Layout B 30928
Polar Log Control Board P	– Circuit Diagram E 32743 – Component Layout B 30929
Amplitude and Correlator Range Control Board R	– Circuit Diagram B 32677 – Component Layout B 31486
Display Board	– Circuit Diagram E 32699 – Component Layout B 30935/6

Correlator Section

Digital Oscillator (Correlator) Board S	– Circuit Diagram B 32744 – Component Layout B 30930
Digital to Analogue Convertor (Correlator) Board T	– Circuit Diagram B 32678 – Component Layout B 30931
Voltage Control (Correlator) Board U	– Circuit Diagram B 32679 – Component Layout B 30932
Analogue to Digital Convertor (Correlator) Board V	– Circuit Diagram B 32680 – Component Layout B 30933

Binary Rate Multiplier Board W	– Circuit Diagram B 32681
Binary Rate Multiplier Boards W and X	– Component Layout B 31488
Binary Rate Multiplier Board X	– Circuit Diagram B 32691

Interconnection Diagrams	– Generator Section B 32687
	– Earthy Section E 32689
	– Correlator Section B 32688

Power Supply Unit	– Circuit Diagram E 32690

SECTION 1

SPECIFICATIONS

1. FREQUENCY RESPONSE ANALYSER SM2001

1.1. Generator Section

(a)	Output Frequency:	(i)	Range: 0.0001Hz to 999Hz in six, decade steps.
		(ii)	Accuracy: 0.01% of setting.
		(iii)	Stability: 20 parts per million per annum (crystal controlled).
		(iv)	Display: 3 side-view numerical indicator tubes with integral decimal points and illuminated units of Hz and Hz x 10^{-3}. Selected by SET F control.
		(v)	Range Selection: 2 front panel push-button controls.
		(vi)	Frequency Selection: 3-pairs of front panel push-buttons or by application of BCD code to rear panel socket, for remote operation.
(b)	Output Amplitude:	(i)	Range: 0V to 10Vp (20V p-p)
		(ii)	Stability: $\pm$ 0.2% short term, $\pm$ 0.2% per annum.
		(iii)	Switched Ranges: 3 ranges, 100mVp, 1Vp, 10Vp.
		(iv)	Display: 3 side-view numerical indicator tubes with integral decimal points, selected by SET V control. Units displayed in mV and V.
		(v)	D.C. Content of Output: 100mV and 1V ranges; $<$100µV. 10V range; $<$1 mV.
(c)	Output Stop/Start:		Controlled by 5 front panel push-buttons. RUN, stop at 0^{o}, 90^{o}, 180^{o}, 270^{o}.
(d)	Output Terminals:		Fully floating, $>$100 MΩ to earth.
(e)	Voltage Proof:		250 V r.m.s., output to chassis.

Correlator Section

(a) Input Impedance: 1 MΩ, ±1% on all ranges.

(b) Frequency Range: 0.00001 Hz to 999 Hz.

(c) Input Terminals: Fully floating, 100 MΩ to chassis.

(d) Dynamic Range of Input Amplifier: 150% of full scale on all ranges.

(e) Measurement Ranges:

(i) Ratio: 4 range positions:
Range 1: full scale for input of 0.01 x generator amplitude on 10V range.
Range 2: full scale for input of 0.1 x generator amplitude on 10V range.
Range 3: full scale for input of 1 x generator amplitude on 10V range.
Range 4: full scale for input of 10 x generator amplitude on 10V range.

(ii) Absolute: 4 range positions: 100mV peak full scale, 1V peak full scale
10V peak full scale
100V peak full scale.

NOTE: 50% overrange provided on all ratio and absolute ranges.

(f) Measurement Accuracy:

(i) *Absolute:*
Cartesian, ±0.5% of reading, ±0.1% scale.

Polar, modulus; ±0.5% of reading, ±0.1% full scale.

Polar, phase angle; ±0.5% of reading at full scale, ±1% at one-tenth full scale.

Log polar, amplitude; ± 0.1dB.

Log polar, phase angle; ±0.5% of reading at full scale, ±1% at one-tenth full scale.

(ii) *Ratio:*
At above 25% generator output; as for absolute (above). At 10% to 25% generator output; ±1% of reading, ±0.2% of full scale.

(g) Correlation: The basic correlation process provides cartesian information, which can be converted to polar and log polar form.

(h) Displays:

Two 4-digit displays (centre and R.H.), using numerical indicator tubes, with integral decimal points to display cartesian, log or log polar co-ordinates;

(i) ***Cartesian:*** Full scale of 1000 with overrange to 1500. Both displays have polarity indication. Units are in V or mV and no units or $x10^{-3}$ (ratio).

(ii) ***Polar:*** The centre display indicates the modulus of the input voltage or ratio and the R.H. display indicates phase angle to 0.1% resolution. Maximum phase angle is 90^{o} and the reference axis is indicated by the quadrant display.

(iii) ***Log Polar:*** Phase angle is displayed as above and modulus is displayed in decibels. This is dB relative to the generator output (Ratio) or relative to 10V peak output (Absolute).

(j) Noise Rejection:

(i) D.C. Series Mode Rejection: >50dB.

(ii) D.C. Common Mode Rejection: >150dB (1k unbalance).

(iii) A.C. Common Mode Rejection (to generator frequency - 1K unbalance): >60dB at 50Hz. >94dB at 1Hz.

(k) Overload indication:

Overload initiated if the input to the correlator exceeds the linear operating range of the system.

(m) Input Overload Protection:

250V r.m.s. on all ranges.

(n) Cycles of Integration:

4-position rotary switch selects cycles of integration from 1 to 1000 cycles in decades.

(p) Harmonic Selection:

Any harmonic up to the 9th can be selected by a 9-position rotary switch. The correlation is then relative to the harmonic and not the fundamental. The upper frequency limit for harmonic measurement is 99.9Hz (99.9kHz with option SM 2003). Cycles of integration are still relative to the fundamental.

(q) Printer Outputs:

Full output information is provided as standard via two 50-way rear panel mounted sockets. Outputs are positive logic and level are standard 7400 TTL.
Outputs are as follows:
Generator Frequency: 3 decades BCD
Frequency Range: 1 decade BCD
Generator Amplitude: 3 decades BCD
Amplitude Range: 3 lines of 1 in n
Correlator Displays: 3 decades of BCD plus overrange digit and polarity for each display, i.e. 30 lines.
Correlator Range: 8 lines in 1 of n.
Display Mode: 3 lines in 1 of n.
Cartesian, Polar and Log Polar.
Integration Cycles: 2 lines of binary.
Harmonic: 1 decade of BCD.
Overload: 1 line
Quadrant: 4 lines 1 of n.
Measurement Complete
(Print Command): 1 line
Zero Voltage Reference: 1 line
Total: 85 lines.

(r) External Programme Facility:

This is fitted as standard and uses one 50 way rear panel mounted plug. All functions are fully programmable. A front panel illuminated latching push-button is fitted and, when this is operated, all programmable manual functions are inhibited. Input logic levels are as for standard 7400 TTL;

Logic 0: −1V to + 0.5V
Logic 1: +1V to +3.6V
Input impedance 1kΩ

Inputs are as follows:−

Generator range:	3 lines 1 of n
Generator Frequency:	3 decades BCD
Frequency Range:	1 decade BCD
Generator Amplitude:	3 decades BCD
Integration Cycles:	2 line binary
Harmonic Selection:	1 decade BCD
Measure:	1 line
Display Mode:	3 lines 1 of n
Correlator Range:	8 lines 1 of n
Total:	49 lines

1.3 **Operating Temperature Range:** $0^{o}C$ to $+50^{o}C$.

1.4 **Power Requirements:**

(i) Voltage Range: 115V, ±15%, or 230V ±15%.

(ii) Frequency Range: 45Hz to 440Hz

(iii) Power Consumption: 150VA (approx.)

1.5 **Dimensions:**

(i) Front Panel: 43.2 cm. x 13.6 cm. (17in x 15¼ in)

(ii) Depth: 63.5 cm. (25 in)

(iii) Weight: 24 kg (53 lb)

1.6 **Optional Accessories:**

(a) Reference Synchroniser SM 2002

This unit consists of two plug-in printed circuit boards which can be purchased separately.
It is used where the system-under-test cannot be excited by the generator output but requires some other source, e.g. mechanical prime mover. A synchronisation signal is provided by the source and taken to rear panel inputs on the frequency response analyser. External synchronisation mode is selected by the front-panel, illuminated, latching push-button and the unit then computes and displays the input frequency in two cycles of the input signal.
NOTE: In this mode, ratio measurements are no longer meaningful.

(b) Frequency Extension Unit SM 2003

This unit extends the frequency range of the SM.2001 by 3 decades to 999kHz and is a free standing unit.
The system employs a slave oscillator and sampling techniques to achieve this high frequency performance. Harmonic measurement is also extended by three decades to 99.9kHz fundamental.

(c) Modulator/Demodulator Unit SM 2004

This unit provides an interface between the SM 2001 and the system-under-test (or components of the system) using a.c. carrier techniques. All connections are via isolating transformers.
The modulator and demodulator sections can be used independently where the system-under-test requires it. Separate carrier sources of different frequency can be used for modulator and demodulator.

SECTION 2

GENERAL INFORMATION

1. INTRODUCTION

1.1. The Frequency Response Analyser SM 2001 (Fig. 2.1.) is designed to measure the frequency response of dynamic systems. Electrical systems can usually be tested directly. Mechanical and Hydraulic systems can be tested using transducers at the outputs and, if necessary, by slaving the generator of the SM 2001 to an external stimulation, using the reference synchroniser SM 2002.

1.2. Frequency response is, in the normal mode, measured by using an internally generated sinewave to excite the system under test, the output of which is measured by the correlator, the results being displayed as:

(a) Quadrature and in-phase component in cartesian form or,

(b) Modulus and phase angle, in polar form or

(c) Log modulus and phase angle in log polar form.

1.3. The correlator measurements, whether in cartesian, polar or log. polar form, can be expressed as an absolute voltage measurement or as a ratio of the input voltage selected, indicating actual system gain. These measurement capabilities allow ***direct*** plotting in Nyquist, Bode or Nicholls form for system design, evaluation and test.

1.4. System non-linearities are totally rejected for measurements of the fundamental selected frequency response. The instrument can, however, select all harmonics up to the ninth and measure the signal content at the selected harmonic, again either in absolute or ratio form.

1.5. An external programming facility is fitted as standard and all functions are fed into the instrument on a 50-way rear panel plug. Also as standard, all the displayed information, including modes and ranges are brought out as outputs on two 50-way rear panel sockets. A front panel illuminated push-button is fitted which when operated, inhibits all manual control functions.

1.6 Digital techniques are used throughout the instrument, ensuring exceptionally high overall stability, resolution and accuracy.

1.7 The instrument can be operated on mains supply voltage of 115 V r.m.s., $\pm$ 15% and 230 V $\pm$ 15%, over a frequency range of 45 Hz to 440 Hz.

FIG. 2 - 1 FREQUENCY RESPONSE ANALYSER SM 2001.

2. OPTIONAL ACCESSORIES

2.1 Reference Synchroniser SM 2002

2.1.1 A reference synchroniser, which consists of two plug-in p.c. boards, can be fitted separately, if required, for use where the system-under-test cannot be excited by the generator output, but requires some other source. A synchroniser signal is provided by the source and taken to rear panel inputs on the instrument. The external sync mode is then selected by an illuminated front panel push-button, and the instrument then computes and displays the input frequency in two cycles of the input signal.

2.2 Frequency Extension Unit SM 2003

This option extends the frequency range of the SM 2001 by three decades to a maximum of 999 kHz. Harmonic measurement is also extended by three decades to 99.9 kHz fundamental.

2.3 Modulator/Demodulator Unit SM 2004

2.3.1 This unit, which uses a.c. carrier techniques, provides an interface between the SM 2001 and the servo system-under-test, so that modulation frequency of the system can be measured. All connections to the SM 2004 are made via isolating transformers, thus minimising problems of common mode signals and earth loops. The modulator and demodulator sections can be used independently where the system-under-test requires it. Separate carrier sources of different frequency can be used for modulator and demodulator.

3. THEORY OF OPERATION

3.1 The SM 2001 consists of two main sections, a generator and a correlator (Fig. 2.2.). The generator section provides the excitation to the system-under-test and the correlator section measures the output of the system (or components of the system), displaying the response relative to the generator output.

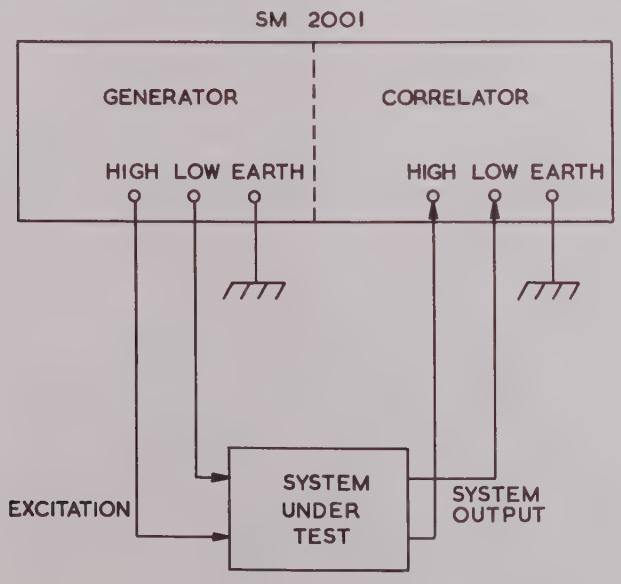


FIG. 2 - 2 CONNECTION TO A SYSTEM.

3.2 Generator Section

3.2.1 The generator section provides a sinewave output, which is derived by a digital process, computing points along the appropriate function. The signal is available in analogue form at the front panel on two fully isolated terminals, having 1000 pF capacity to ground. This allows application of the excitation across any two points of the system-under-test, neither of which need be earthed. A total of 1024 points are computed for each sinewave period and the frequency is controlled from a crystal source. The generator section can be stopped and started at any quadrant point.

3.2.2 Amplitude stability of the excitation sinewave is determined by the reference source and precision resistors in the digital-to-analogue (D/A) converter, these circuits being independent of frequency sensitive components. The amplitude, once set during a measurement, to a suitable level, is held constant throughout the frequency response test. Alteration of the generator section frequency does not cause transients that could damage or overload the system-under-test, although a change in frequency will cause a slope change in the output waveform.

3.2.3 The frequency available from the basic SM 2001 ranges from 0.00001 Hz to 999 Hz (and up to 999 kHz with option SM 2003). The sinewave is digitally synthesised so that the d.c. component of the output is very small. Also, as the correlation process is digital and the digital timing waveforms (nW-CosnWt) must be related to the generator, the digitally synthesised generator output is essential.

3.2.4 The generator section (fig. 2.6) consists of three main areas, a master digital oscillator, voltage (amplitude) digital-to-analogue converter and a sine digital-to-analogue converter. The signals controlling the generator section are derived from frequency and voltage control logic.

3.2.5 *Sinewave Generation:* A simplified block schematic of the generator section is shown in fig. 2.3. The master digital oscillator utilises two four-bit binary rate multipliers, one feeding a ten-bit synchronous down-counter and the other a ten-bit synchronous up-counter, the length of count keeping the distortion (deviation from a true sinewave) to less than $\pm$ 0.5%. The digital oscillator only generates one quadrant.

3.2.6 The quarter-cycle information is used to select which counter output is fed through to the D/A converter. From this, half-cycles are generated and this information is used to invert alternate half-cycles, the final result being a complete sinewave. This output is fed via an amplitude attenuator (controlled from the front panel) and a buffer stage to the generator section output terminals.

3.2.7 *Sinewave Frequency Control:* The output from the frequency control circuit (fig. 2.4) is derived from three decade rate multipliers (DRM) feeding into range dividers. The rate output from each DRM is controlled by the value set into the associated synchronous up/down decade counter by operation of the UP:DOWN push-buttons on the front panel. These values are also displayed by the generator section display, provided that the SET F push-button has been depressed.

3.2.8 The range dividers, which accept the outputs from each DRM, are also controlled by a synchronous decade up/down counter, the output of which is decoded to give a ten-line output, that in turn, gates the outputs of the range dividers. This decade UP/DOWN counter is controlled by the FREQUENCY RANGE push-buttons on the front panel.

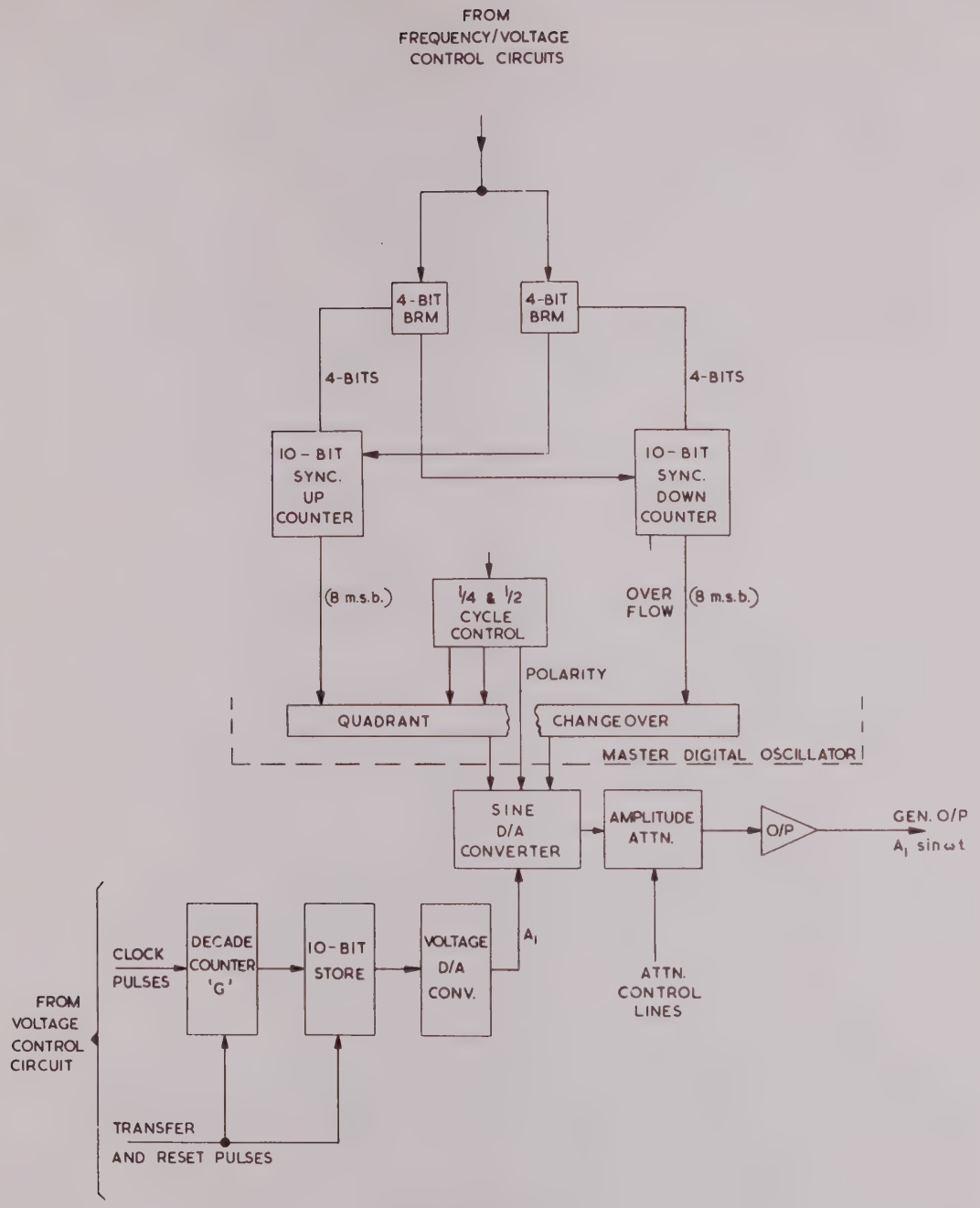


FIG. 2 - 3 SINEWAVE GENERATION - BLOCK SCHEMATIC

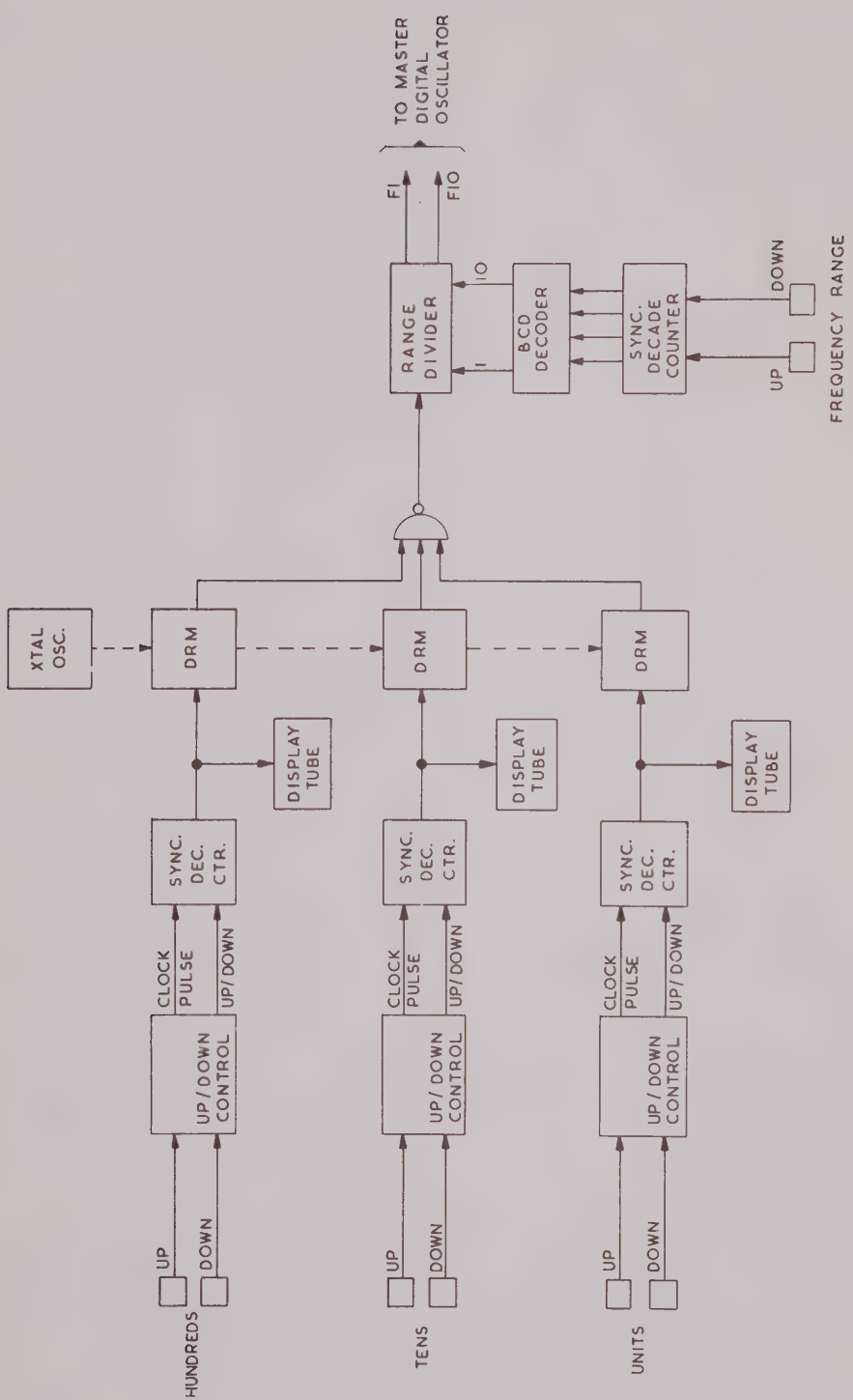


FIG. 2 - 4 SINEWAVE FREQUENCY CONTROL - BLOCK SCHEMATIC

3.2.9 *Sinewave Amplitude Control:* A block schematic of the voltage amplitude control circuit is shown in fig. 2.5. Clock pulses are fed into the decade counters A, B and C and also into the voltage D/A converter (via the control logic). The value of the outputs produced by the synchronous decade counters D, E and F is set by operation of the front panel UP:DOWN push-buttons. When the comparator circuit detects that the decade counters A, B and C contain the same values as synchronous counters, D, E and F (i.e. parity is reached), a transfer and reset pulse is generated.

3.2.10 The clock pulses fed into the voltage D/A converter are counted by another decade counter G (fig. 2.3) and when parity is reached, the count is transferred (by the pulse generated above) to the ten-bit store. The output of the store controls the voltage D/A converter output, A.

3.2.11 This sequence is repeated each time the decade counters A, B and C are reset (i.e. parity no longer exists). In this way, the voltage D/A converter is continually updated.

3.3 Correlator Section

3.3.1 The correlator section accepts the output from the system-under-test, which has both terminals fully floating. This input is converted into digital form and is then multiplied by both the sine reference (which is in-phase with the generator excitation signal) and the cosine reference (in quadrature with the excitation signal). The resulting products are then integrated over a pre-set number of cycles (set-in by a front-panel control).

3.3.2 At the end of the integration period, the integrators contain the cartesian components of the output signal with respect to the reference. The degree to which unwanted harmonics and interference is eliminated depends on the number of cycles over which integration takes place (as set-in by a front panel control). As the multiplication and integration processes are performed digitally, the accuracy is high.

3.3.3 The correlator section is shown in fig. 2.6. The input A/D converter produces 8-bit, binary, parallel information which is then multiplied by the serial sine and cosine pulse rates, by the binary rate multipliers. Quadrant information and polarity is deduced from the zero-crossing of the input wave form and the zero crossings of the reference sine and cosine waveforms.

3.3.4 The multiplier rate outputs are fed to the harmonic selection circuit where they are divided by the harmonic value as set-in by a front panel control. Fig. 2.6 shows the mathematical values of the multiplier outputs which contain the harmonic-under-measurement, 'n', and this multiplying factor must be removed before integration takes place.

3.3.5 Absolute measurements are made, using a fixed reference voltage (Vref) derived from the voltage amplitude D/A converter, and fed to the input A/D converter. For ratio measurements, the reference voltage (A_1) is the same as that of the generator section (in value only, as they are electrically isolated).

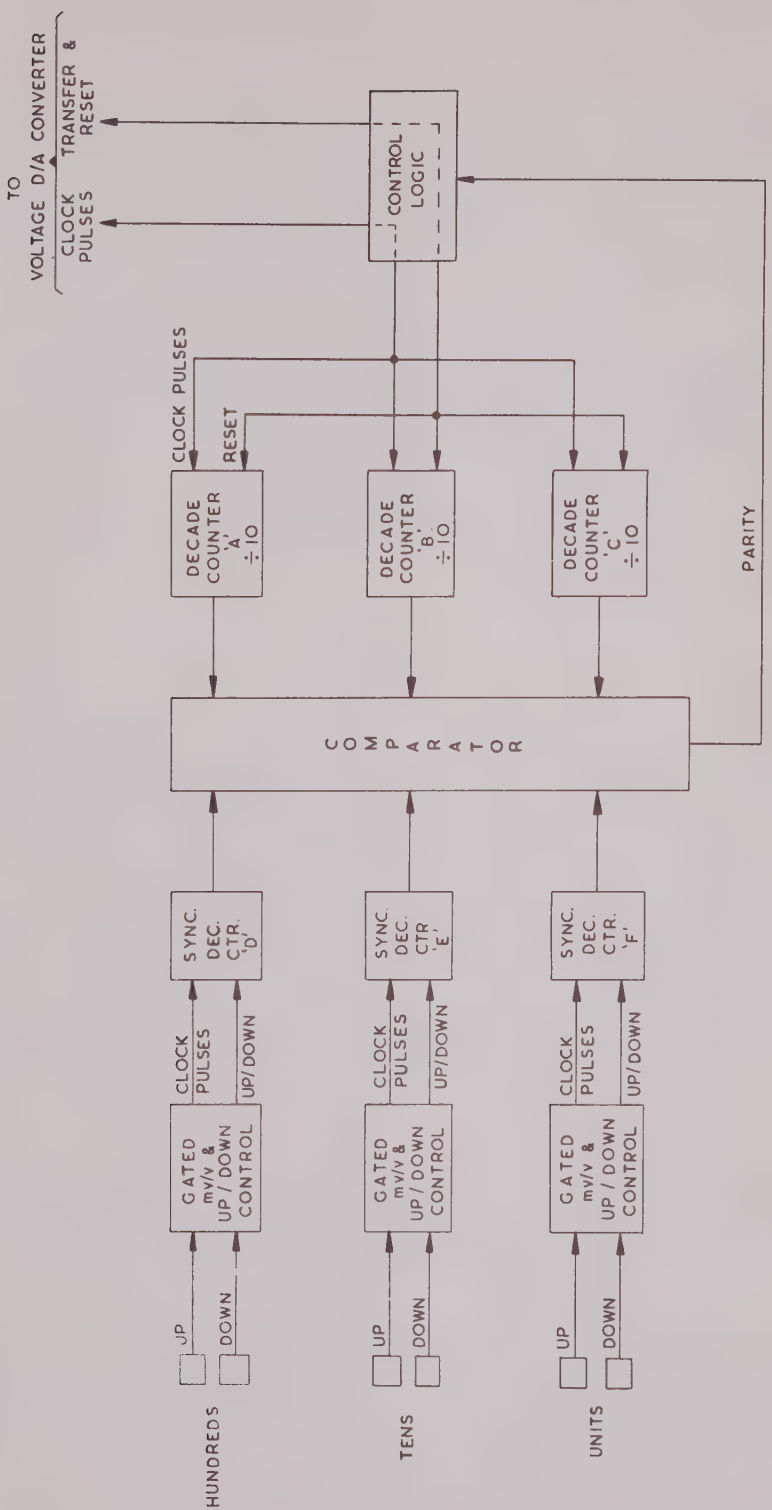


FIG. 2 - 5 SINEWAVE AMPLITUDE CONTROL - BLOCK SCHEMATIC

3.3.6 *Integration and Conversion.* The output from the harmonic selection circuit passes to the integrators via an integration cycles circuit that divides the rates by 1,10,100 or 1000 (as set by a front panel control). This effectively reduces the bandwidth of the measurement in proportion to the number of cycles of integration. Large signals at frequencies close to the measurement frequency can be 'integrated out'. The result is displayed by numerical indicator tubes in cartesian form. The polarity is also displayed so that the quadrant of the input signal, with respect to generator output, can be deduced.

3.3.7 The cartesian co-ordinates can be displayed indefinitely or converted to polar (R,θ) form (modulus and phase angle). The phase angle is always referred to the rear axis, so that the displayed phase angle is 90^{o} or less. In the polar mode, the quadrant indicator is illuminated and from this, the position of the modulus vector can be found. Further conversion turns the R (modulus) value into polar log form and the result is then $20 \log_{10} R$.

3.3.8 With absolute measurements, the values displayed are as voltage and phase angle. Ratio measurements produce results as a numerical value and phase angle. No dimensions are assigned.

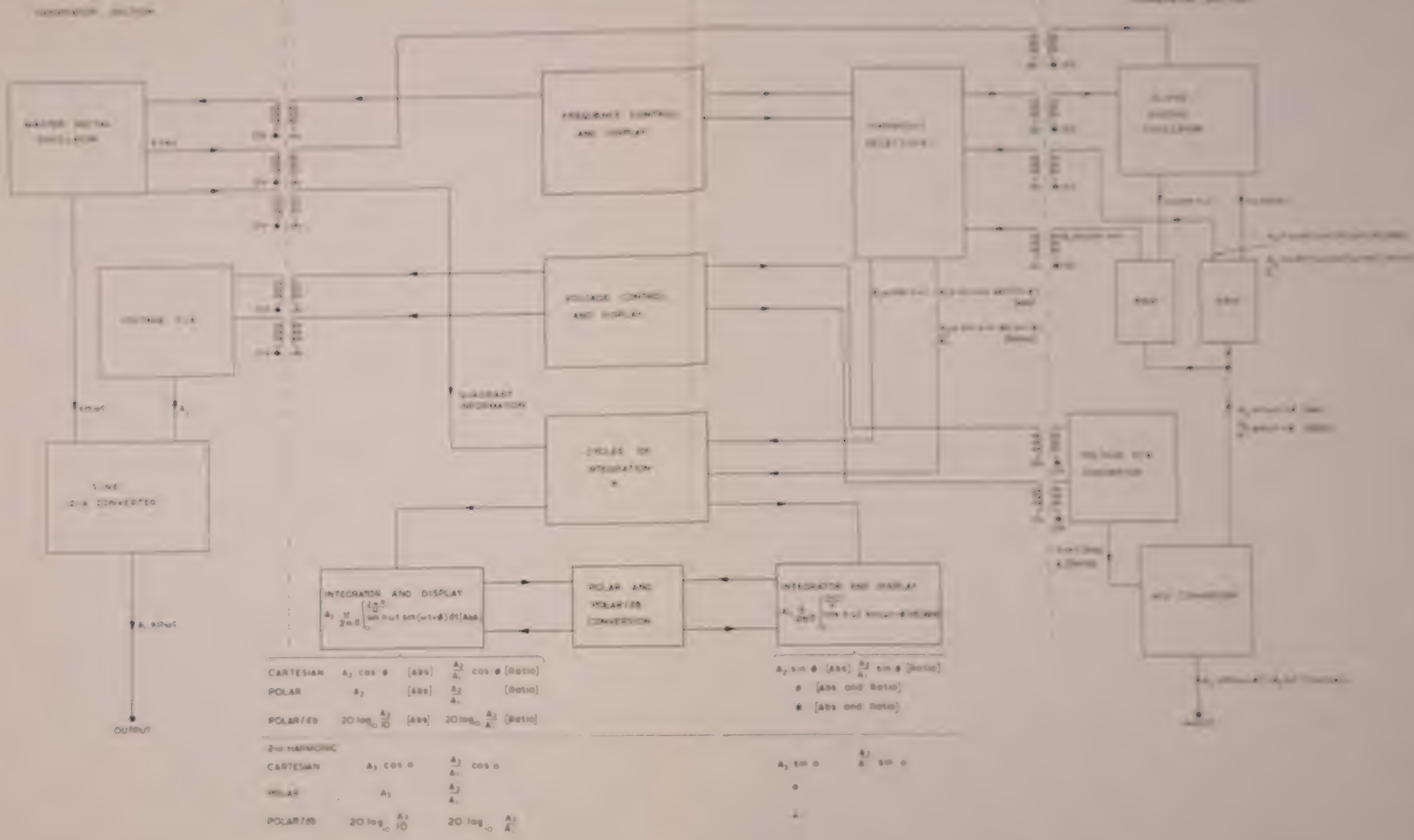

INTEGRATOR AND DISPLAY
POLAR AND POLAR/DB CONVERSION
INTEGRATOR AND DISPLAY
CARTESIAN
POLAR
POLAR/db
2nd HARMONIC
CARTESIAN
POLAR
POLAR/DB
OUTPUT

FIG. 2-6

SECTION 3

INSTALLATION AND OPERATION

1. INTRODUCTION

1.1 This section contains all the information necessary to install and operate the Frequency Response Analyser SM 2001.

2. UNPACKING

2.1 The instrument is supplied sealed in a polythene bag and is surrounded by rubber packing blocks. These should be retained for use again if further transportation is likely.

3. EQUIPMENT CHECK LIST

(a)	Frequency Response Analyser SM 2001	
(b)	50-way Plug, McMurdo, MP 150 with Cover, End Entry Type, MC 150C – 1 off.	
(c)	50-way Socket, McMurdo, MS 150, with Cover, End Entry Type, MC 150C – 2 off.	
(d)	Instruction Manual	1 off
(e)	Rack Mounting Kit SM 2001R	(Optional)
(f)	Reference Synchroniser SM.2002	(Optional)
(g)	Frequency Extension Unit (x1000) SM 2003 with interconnection cable (Optional)	
(h)	Modulator/Demodulator Unit SM 2004, with interconnection cable (Optional)	

4. RACK MOUNTING

4.1 The SM 2001 can be bench or rack mounted. A system of rack sliding supports is fitted along the sides of the instrument and extensions are added to either side of the front panel so that it can be held in place on the rack. This system is available in kit form as an optional extra.

5. MAINS (POWER) SOURCE CHECKS

5.1 The instrument can be operated on mains voltages of 115V r.m.s., ± 15% and 230 V r.m.s., ± 15% and between mains frequencies 45Hz to 440Hz. A label is attached to the instrument denoting the mains voltage to which the instrument has been set. This should be checked.

5.2 To alter the mains setting to agree with the local mains source, a system of links must be altered on a special tagstrip mounted internally at the rear of the instrument. It is advised that this task is performed by S.E. Laboratories personnel only.

5.3 Connect a suitable plug to the mains lead:

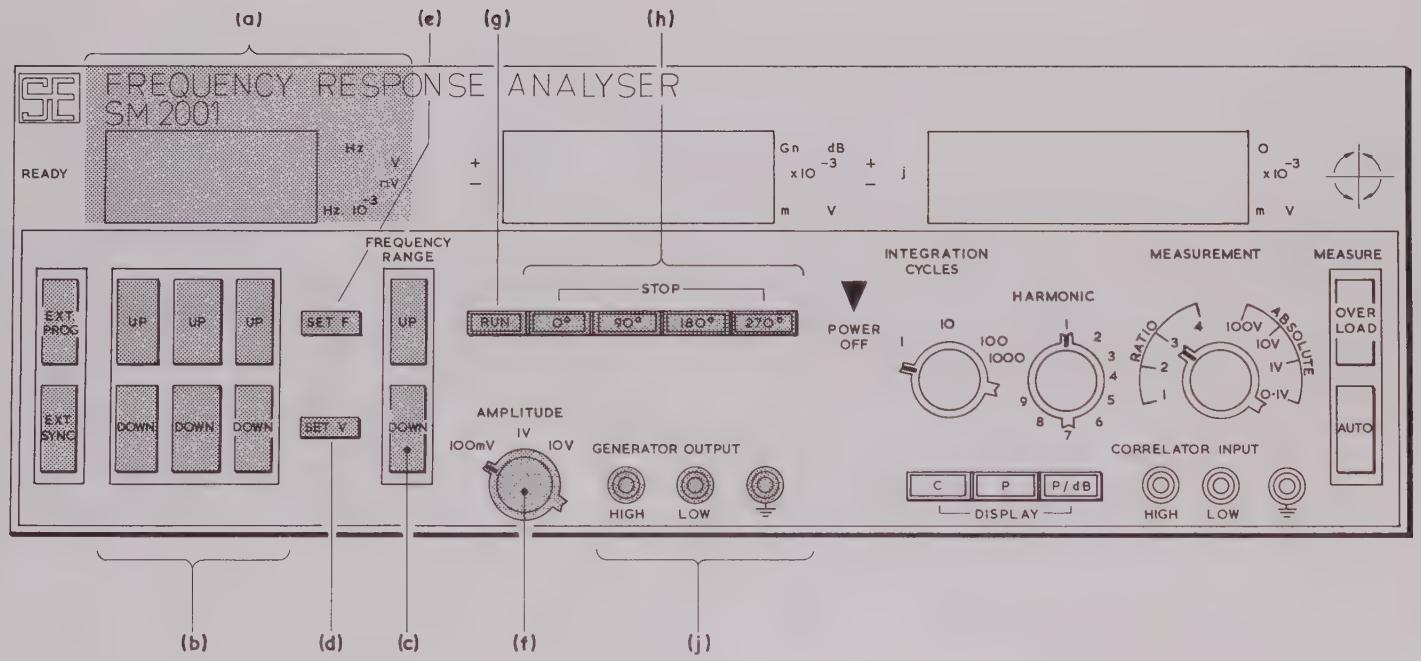
Colour	Function
Brown	LIVE
Blue	NEUTRAL
Green/Yellow	EARTH (GROUND)

5.4 Check that a fuse is inserted in the fuseholder on the rear panel. The value of this fuse should be 1A antisurge for 230V mains, and 2A antisurge for 115V mains. On certain models two mains fuses are fitted, one in the 'live' line and one in the 'neutral' line.

6. SUMMARY OF CONTROLS, CONNECTORS AND INDICATORS

6.1 Generator Section (Fig. 3.1)

(a)	Generator Display	Three digit display provided by side-view numerical indicator tubes with integral decimal points, which can display frequency or voltage amplitude as selected by the SET F and SET V push-buttons. For frequency, units in Hz and Hz x 10^{-3} are displayed. For voltage amplitude, units in-V and mV are displayed. (see below for associated controls).
(b)	Generator Output Push-buttons	Identified as a group of 3 pairs of orange and white UP : DOWN push-buttons, each pair of which changes the number displayed in the indicator tube immediately above it, up or down (either frequency or voltage amplitude, dependent upon positions of SET F and SET V push-buttons). If either push-button is held down, the display will cycle at 2Hz, so that values can be set quickly, in the direction selected.
(c)	FREQUENCY RANGE push-buttons	Identified as a single pair of orange and white push-buttons to the R.H. side of the SET V/SET F push-buttons. These control the frequency range of the generator display, and control the position of the decimal point.
(d)	SET F push-button	When depressed, selects the generator display to indicate frequency.
(e)	SET V push-button	When depressed, selects the generator display to indicate voltage.
(f)	Amplitude selector	3-position rotary switch that selects the full scale range of the generator display, when set to indicate voltage amplitude. Interpolation between these positions is by use of the 3 pairs of UP DOWN push-buttons located immediately below the display, (as in (b) above).
(g)	RUN push-button	When depressed, starts the generator output waveform.
(h)	STOP:0^{o}, 90^{o}, 180^{o}, 270^{o} push-buttons	4 quadrant push-buttons, used in conjunction with the RUN push-button. Pressing any one causes the



(a) GENERATOR DISPLAY

(b) GENERATOR OUTPUT PUSH-BUTTONS

(c) FREQUENCY RANGE PUSH-BUTTONS

(d) SELECT FREQUENCY (SET F) PUSH-BUTTON

(e) SELECT VOLTAGE (SET V) PUSH-BUTTON

(f) AMPLITUDE (RANGE) SELECTOR

(g) RUN PUSH-BUTTON

(h) QUADRANT PUSH-BUTTONS

(j) GENERATOR OUTPUT TERMINALS

FIG. 3-1 GENERATOR SECTION-CONTROLS AND INDICATORS

waveform to stop when it reaches the quadrant point engraved on the button.

(j) GENERATOR OUTPUT terminals

The HIGH and LOW terminals are fully floating, greater than 100 MΩ to ground. The earth terminal is connected to chassis (line ground).

6.2 Correlator Section (Fig. 3.2)

(a) CORRELATOR INPUT Terminals

The signal to be measured is connected to the HIGH and LOW terminals. The input is fully floating, isolation $>$100MΩ to ground. Input impedance 1MΩ on all ranges. The earth terminal is connected to chassis (line ground).

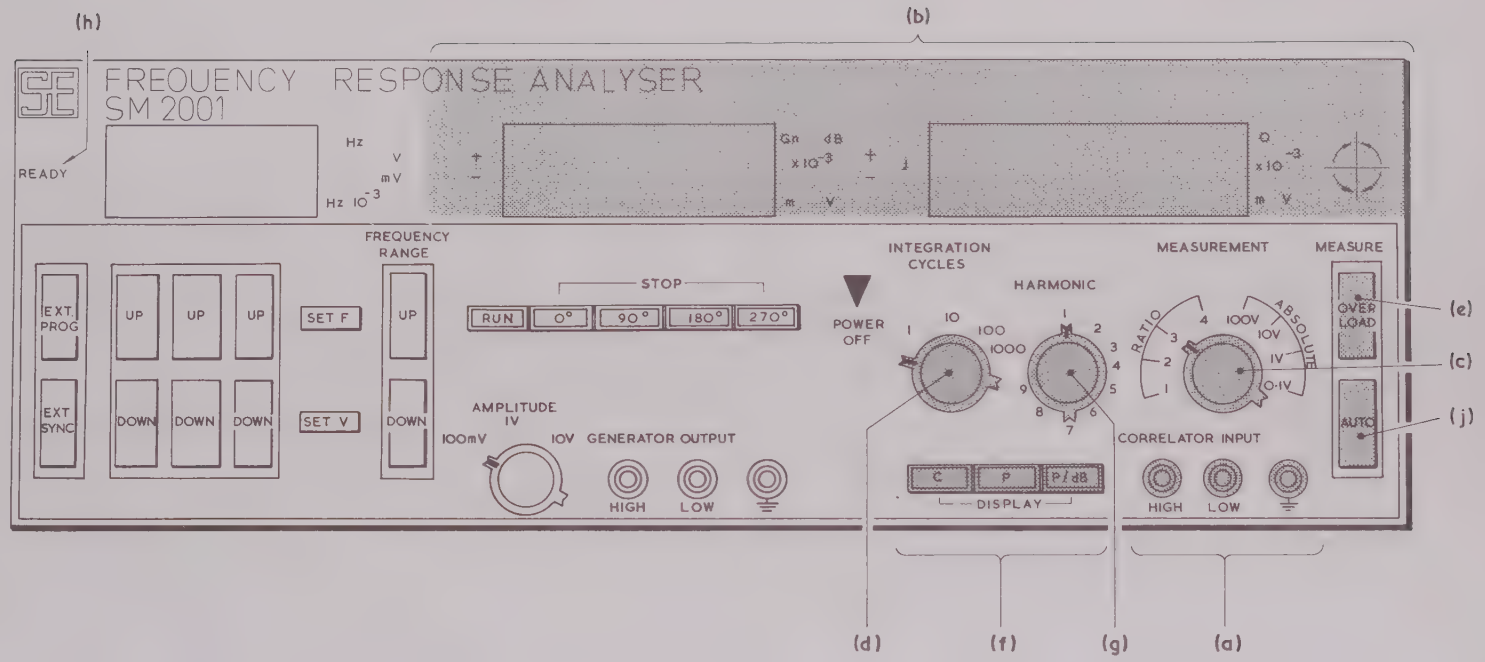
(b) Correlator Displays

(i) Cartesian Display
Two 4-digit displays using side-view numerical indicator tubes. Full scale of 1000 with overrange to 1500. Both displays have polarity indication and switched decimal points. Units are V and mV (in absolute mode) and no units or $x10^{-3}$ (in Ratio mode).

(ii) Polar Display
In this display mode, the centre display indicates the modulus of the input voltage or ratio, and the R.H. display indicates phase angle (to 0.1 degree resolution). Maximum phase angle indication is 90 degrees and the quadrant display indicates the reference axes.

(iii) Log Polar Display
In this display mode, the phase angle is displayed on the R.H. display. The centre display indicates the modulus in decibels, relative to Generator Section output (in ratio mode) or relative to 10V peak (in absolute mode).

(iv) Quadrant Display
Located immediately to the right of the R.H. display, phase angle quadrants 1 to 4 are indicated in the Polar and Log Polar modes, moving in anti-clockwise direction.



(a) CORRELATOR INPUT TERMINALS

(b) CORRELATOR DISPLAY

(c) MEASUREMENT SELECTOR

(d) POWER AND INTEGRATOR CYCLES SELECTOR

(e) MEASURE PUSH-BUTTON/OVERLOAD LAMP

(f) DISPLAY PUSH-BUTTONS

(g) HARMONIC SELECTOR

(h) READY INDICATOR

(j) AUTO PUSH-BUTTON

FIG. 3-2 CORRELATOR SECTION - CONTROLS AND INDICATORS

(c) MEASUREMENT Selector:

8-position rotary switch, having 4 RATIO ranges and 4 ABSOLUTE ranges. This selector adjusts the sensitivity of the correlator to suit the amplitude of the input signal. It should be set to provide the greatest resolution of display.

Ratio Ranges

4 Ratio ranges are provided for use where gain measurements are required, the reading being in terms of gain:

Range 1: Full scale for an input of 0.01 times the Generator's AMPLITUDE setting on 10V range

Range 2: Full scale for an input of 0.1 times the Generator's AMPLITUDE setting on 10V range

Range 3: Full scale for an input of 1 times the Generator's AMPLITUDE setting on 10V range

Range 4: Full scale for an input of 10 times the Generator's AMPLITUDE setting on 10V range

Note: No multiplication factors are required since the decimal points of the correlator's display are switched according to the Generator & Correlator range settings.

Absolute Ranges

100V Range: Up to full scale of 100V peak can be displayed.

10V Range: Up to full scale of 10V peak can be displayed.

1V Range: Up to full scale of 1V peak can be displayed.

0.1V Range: Up to full scale of 100mV peak can be displayed.

Note: 50% overrange is provided on all ranges of RATIO and ABSOLUTE measurements.

(d) POWER OFF/INTEGRATION CYCLES Selector:

5-position rotary switch with positions as follows:

POWER OFF to 1 : This switches on the instrument and at the same time selects 1 cycle of integration time of the correlator.

10, 100, 1000: Each numbered position denotes the number of cycles over which integration takes place.

(e) MEASURE pushbutton/OVERLOAD Indicator:

A combined indicator and push-button control used as follows:

(i) Measure select (indicator unlit). When depressed, initiates the measurement sequence. The correlator's display is blanked during the measurement period.

(ii) Overload Indication and Reset. This indicator is illuminated when any part of the correlator is driven into saturation. This occurs irrespective of whether the instrument is measuring or not. Depressing the push-button resets the overload lamp (provided the cause of the overload has been rectified).

(f) DISPLAY push-buttons:

The instrument always measures the in-phase component and the quadrature component of the correlator input:

(i) C Push-button: With this push-button depressed, the measured result is displayed in two display windows (centre display and the R.H. display). The in-phase component is displayed on the centre display and the quadrature component on the R.H. display.

(ii) P Push-buttons: With this push-button depressed, the reading in (i) above is converted into polar form. The centre display reads amplitude and the R.H. display reads phase angle (to 0.1^{o} resolution). The quadrants are defined by the 'arrowed' quadrant indicator immediately to the right of the R.H. display.

(iii) P/dB Push-button: With this push-button depressed, the amplitude term is converted into logarithmic form. The centre display reads log polar, referred to a base of zero dB, equal to 10V.

(g) HARMONIC selector:

9-position rotary switch is provided for measuring individual harmonics up to the 9th on all frequency ranges except 999Hz range. The switch selects the harmonic to be measured and the results are measured relative to the fundamental frequency.

(h) READY Indicator

This lamp (located extreme left of the generator's display) indicates when the instrument is ready to make a measurement.

(j) AUTO Push-button:

When depressed, the readings are automatically taken with an approximate display time of 1 second between readings.

The push-button is illuminated when in operation, and is located below the MEASURE push-button.

6.3 External Mode Facilities (Fig. 3.3)

(a)	EXT PROG Push-button:	Front panel illuminated push-button, when operated all programmable manual functions are inhibited and the instrument can be remotely programmed. In this mode, control of the generator section and correlator section is exercised by external commands which are fed into the instrument on a rear panel connector (see Para. 7.5. External Programme Facility).
(b)	EXT SYNC Push-button:	Front panel illuminated push-button, operable only when Reference Synchroniser SE.2002 is fitted to the instrument, and the system under test cannot be excited by the output of the Generator Section, but requires an external source. A sync signal is provided by the source and fed to the instrument via a rear panel input connector. Operating the EXT SYNC push-button selects the external sync mode and the instrument computes and displays the input frequency in 2 cycles of the input signal. NOTE: In this mode, ratio measurements have no meaning.
(c)	Rear Panel Connectors	(i) Two 50-way McMurdo sockets (printer output) (ii) 50-way McMurdo plug (external programme)

7. OPERATING INSTRUCTIONS

7.1 Initial Checks and Familiarisation

7.1.1 These checks are intended to check-out the operation of the instrument and to help with familiarisation.

7.1.2 The user is recommended to refer to Para. 6, Summary of Controls, Connectors and Indicators, before attempting to operate the instrument:-

(a) Ensure that the instrument has been correctly set for the local mains (power) source and that a suitable plug has been fitted to the mains cable (see Para. 5, Mains (Power) Source Checks).

(b) Set the POWER OFF/INTEGRATION CYCLES selector to 1. Depress the RUN push-button.

(c) Check that the EXT PROG push-button is not operated, i.e. not lit.

(d) Check that the EXT SYNC push-button is not operated, i.e. not lit.

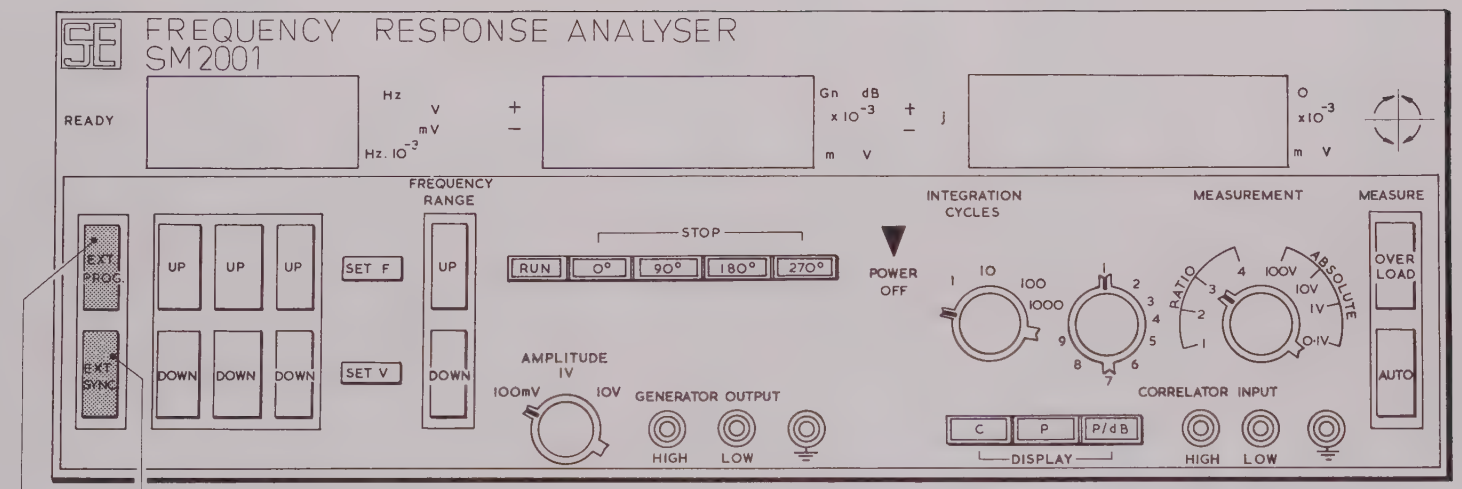
(e) Set the Generator Section output frequency to 20Hz as follows:

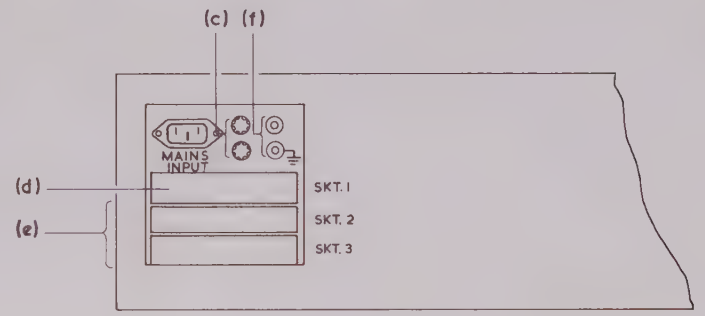
(i) Depress SET F.

(ii) Operate (single pair) of coarse FREQUENCY RANGE push-buttons to position the decimal point in the R.H. tube of the generator display.

(iii) Operate each pair of fine range push-buttons until the generator display indicates 20.0Hz.

Note: On some early models, Frequency Range may occasionally 'lock out' for a non-permitted state following Power On. If this occurs, operating and releasing the EXT SYNC push-button will select the lowest frequency range.





REAR PANEL

(a) EXTERNAL PROGRAM PUSH-BUTTON

(b) EXTERNAL SYNC. PUSH-BUTTON

(c) FUSES (1A FOR 230V OR 2A FOR 115V)

(d) EXTERNAL PROGRAM (MALE) CONNECTOR SKT 1

(e) PRINTER OUTPUT (FEMALE) CONNECTORS SKT 2 & 3

(f) EXTERNAL SYNC. INPUT TERMINALS

FIG.3·3 EXTERNAL MODE FACILITIES

(f) Set the Generator Section output voltage amplitude to 9V as follows:

(i) Depress SET V.
(ii) Set AMPLITUDE TO 10V.
(iii) Operate each pair of the fine range UP:DOWN push - buttons until the generator display indicates 09.0V.

(g) Set the correlator MEASUREMENT selector to ABSOLUTE 10V, and HARMONIC selector to 1.

(h) Connect the output terminals of the generator section to the input of the correlator section (High to High, Low to Low).

(j) Depress the correlator DISPLAY C push-button.

(k) Set the INTEGRATION CYCLES selector to 10.

(m) Depress the RUN push-button.

(n) Allow a 5-minute warm-up time to elapse and then depress the MEASURE push-button. The following sequence should result:

(i) All displays cleared to zero and are extinguished (this occurs at the first quadrant point of the waveform).
(ii) READY indicator extinguished.
(iii) 0.5 second delay.
(iv) Displays present measurement reading. The centre display should read +09.00V $\pm$ 00.04V and the R.H. display should read 00.00, $\pm$ 00.03V.

(p) Depress the correlator DISPLAY P push-button. The centre display should read +09.00V, $\pm$ 00.04V. and the right hand display should read 000.0°, $\pm 000.3^{\circ}$. Quadrants 1 or 4 should be illuminated.

(q) Depress the correlator DISPLAY P/dB push-button. The R.H. display should read as in (p) above, and the centre display should read −001.0dB, $\pm$ 000.1dB. Depress the MEASURE push-button and check that the readings return to the same values.

7.2 Taking a Measurement

(a) Connect the input of the system-under-test to the Generator Section output terminals (HIGH and LOW) and connect the signal-to-be-measured to the Correlator Section (HIGH and LOW) terminals.

(b) Set the generator output frequency to the desired test frequency.

(c) Set the generator output voltage to the approximate desired test level.

(d) Set the number of cycles over which integration is to take place.

(e) Set the MEASUREMENT selector to the expected range (and mode required) of the signal-to-be-measured.

(f) Set the correlator displays to indicate cartesian, polar or polar dB as required.

(g) Depress the MEASURE push-button. After the measurement period has elapsed, the result is displayed. If the OVERLOAD indicator lights up during or after the measurement period, the measurement selector should be set to a higher range and the measuring sequence repeated. If the result is less than one tenth of full scale, the MEASUREMENT selector should be set to a lower range and the measuring sequence repeated.

(h) To measure and display as log polar, measure in the polar mode initially and then convert to Log Polar. This checks that the measurement selector is set within the limits described in (g) above. Alternatively, it is necessary to ensure that the MEASUREMENT selector is set to the following positions for a result within the corresponding range (see Tables 3.1 and 3.2);

NOTE: The conversions to polar and log polar each take less than 1 second.

MEASUREMENT (Absolute) Position	Log Polar Range Limits
0.1V	−60dB to −40dB
1V	−40dB to −20dB
10V	−20dB to 0
100V	0 to +20dB

TABLE 3.1

Generator AMPLITUDE selector position	MEASUREMENT (Ratio) Position	Log Polar Range Limits
100mV	1	−20dB to 0
100mV	2	0 to +20dB
100mV	3	+20dB to +40dB
100mV	4	+40dB to +60dB
1V	1	−40dB to −20dB
1V	2	−20dB to 0
1V	3	0 to +20dB
1V	4	+20dB to +40dB
10V	1	−60dB to −40dB
10V	2	−40dB to −20dB
10V	3	−20dB to 0
10V	4	0 to +20dB

TABLE 3.2

(j) To measure up to the 9th harmonic on all fundamental frequency ranges except 999 Hz:

(i) Measure the fundamental (HARMONIC selector on 1) and obtain a reading as near full scale as possible (as a signal with a low harmonic content will give a low reading on the harmonic position). For example, a distortion of 1% would give a reading 0010 if the fundamental reading was 1000.

(ii) Set the HARMONIC selector to the harmonic required and select the type of display required.

NOTE: An OVERLOAD condition will result if too much sensitivity is applied, the fundamental component overloading the instrument's input amplifier.

7.3 Phase Angle Measurement

7.3.1 The correlator section always measures the in-phase component and quadrature component with respect to the Generator Section output. The phase angle is then computed by a digital process from the values of these components. The limits of phase measurement accuracy are set by the quantization of the measured components. Each component is resolved into the nearest number in a scale which increases with equal steps of a given value.

7.3.2 For example, with an in-phase component of 999 (full scale) and a quadrature component of 001, the phase angle is $1/20^{o}$, which is the smallest angle that can be resolved. If the in-phase component is changed to 099 (one tenth of full scale), the phase angle is $Tan^{-1}\ 1/99 = 1/2^{o}$ approximately. Thus, a one bit error in the quadrature reading can give a $1/2^{o}$ error at one tenth of the full scale amplitude.

7.3.3 The polar converter has similar errors. A conversion has a maximum error of 0.5^{o}, when the amplitude is at full scale, which increases linearly to less than 1^{o} at one tenth of full scale amplitude.

7.3.4 Where a precise phase measurement is required, the amplitude of the Generator Section output (or external excitation source) should be adjusted so that the amplitude of the signal-to-be-measured is greater than one half of full scale.

7.3.5 The phase accuracy ($\pm$0.5% at full scale and $\pm$1% at one tenth full scale) is the same for all ranges, so that full scale readings are obtained either by increasing the Generator Section output (or external excitation source) on one range or by decreasing the Generator Section output level and switching the correlator to a lower voltage range.

7.3.6 At full scale, the phase measurement capability is $1/20^{o}$ in cartesian and 0.5^{o} in polar.

7.3.7 *Phase Measurement Accuracy Check*

(a) Make-up a circuit as shown in Fig. 3.4. The value of R1 should be about 1 kΩ and the capacitor C1 greater than 0.1 μF.

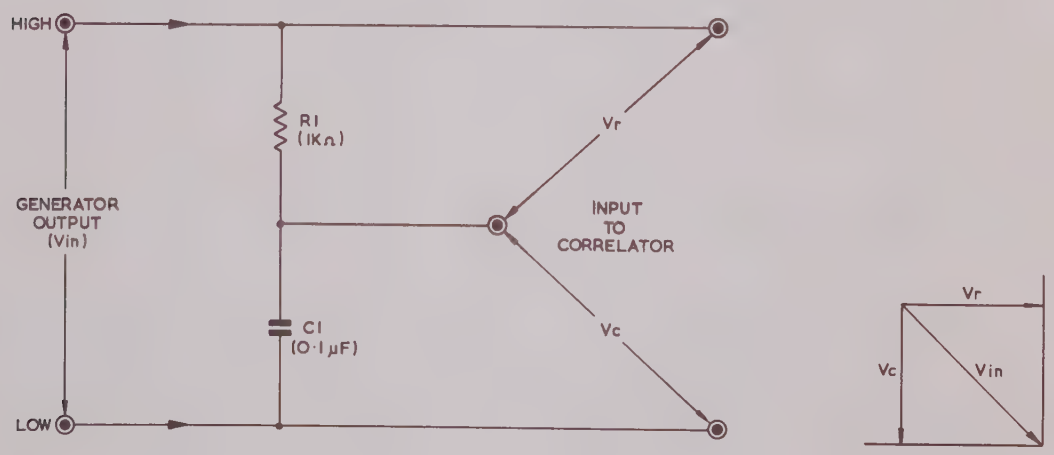


FIG. 3.4 PHASE MEASUREMENT CHECK

(b) Connect the generator output terminals across the circuit.

(c) Connect the Correlator input terminals across R1 and C1 in turn. The difference in phase readings should always be 90^{o} (or 270^{o}) depending upon which way the circuit is connected to the correlator. The accuracy depends upon the generator amplitude setting. Errors should be less than 1^{o} at one tenth full scale amplitude and less than 0.5^{o} at full scale amplitude.

7.4 Printer Output Facility

7.4.1 Full printer output information is available in digital form on two 50-way rear mounted sockets. The state (or position) of a control is indicated by the logical state of certain outputs on those sockets. The Generator Section output is also available in digital form (BCD). All outputs are positive logic and levels are as for standard Texas 7400 series integrated circuits: Logic 1: +2.4V min to +5V max.
Logic 0: 0 to +0.4 max, sink capability 10mA.

The socket pin connections, codes and operative levels are listed below:

(a) Generator Frequency O/Ps (SKT 2)

HUNDREDS Pin Nos.	TENS Pin Nos.	UNITS Pin Nos.	BCD Code
C7	C6	C5	8
B7	B6	B5	4
A7	A6	A5	2
D6	D5	D4	1

(b) Generator Frequency Range O/Ps (SKT 2)

RANGE	Pin Nos. D7	A8	B8	C8
1	0	0	0	1
2	1	0	0	1
3	0	0	0	0
4	1	0	0	0
5	0	1	0	0
6	1	1	0	0

(c) Generator Voltage O/Ps (SKT 2)

HUNDREDS Pin Nos.	TENS Pin Nos.	UNITS Pin Nos.	BCD Code
D3	D2	D1	8
C3	C2	C1	4
B3	B2	B1	2
A3	A2	A1	1

(d) Generator Voltage Range O/Ps (SKT 2)
1 of n Code

RANGE	Pin Nos. A4	B4	C4
100mV	1	0	0
1V	0	1	0
10V	0	0	1

(e) *Cycles of Integration O/Ps (SKT 2)*

CYCLES	Pin Nos.	
	D8	A9
1	0	0
10	1	0
100	0	1
1000	1	1

(f) *Harmonic O/Ps (SKT 2)*

Harmonic	Pin Nos.			
	B9	C9	D9	A10
Fundamental	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

(g) *Print Inhibit O/P (SKT 2) - B10*
Logic 0 for Print.

(h) *Correlator Range O/Ps (SKT 2)*
1 of n code

RANGE O/P	0.1V Abs	1V Abs	10V Abs	100V Abs
Pin	C10	D10	A11	B11
RANGE O/P	10R	1R	0.1R	0.01R
Pin	C11	D11	A12	B12

(j) *Display Mode O/Ps (SKT 2)*
1 of n code

MODE	Pin No.
Cartesian	C12
Polar	D12
Polar dB	A13

(m) *Clock O/P (6.74 MHz)* SKT 3 - A1

(n) *Generator ¼ Cycle O/P* SKT 3 - B1

(p) *Generator ½ Cycle O/P* SKT 3 - C1

(q) *Control Lines from SM 2003* SKT 3 - D1 and A2

(r) *Overload Output* SKT 3 - B2

(s) *Sine Register O/Ps* SKT 3

THOUSANDS Pin No.	HUNDREDS Pin Nos.	TENS Pin Nos.	UNITS Pin Nos.	BCD Code
–	B5	B4	B3	8
–	A5	A4	A3	4
–	D4	D3	D2	2
C5	C4	C3	C2	1

(t) *Sine Register Polarity O/Ps - SKT 3*

Positive	D5
Negative	A6

(u) *Cosine Register O/Ps - SKT 3*

THOUSANDS Pin No.	HUNDREDS Pin Nos.	TENS Pin Nos.	UNITS Pin Nos.	BCD Code
–	A9	A8	A7	8
–	D8	D7	D6	4
–	C8	C7	C6	2
B9	B8	B7	B6	1

(v) *Cosine Register Polarity O/Ps - SKT 3*

Positive	C9
Negative	D9

(w) *Correlator Quadrant O/Ps - SKT 3*
1 of n code

Quadrant	Pin No.
1	A10
2	B10
3	C10
4	D10

(x) *Zero volt reference* SKT 3 - C13

7.5 External Programme Facility

7.5.1 The instrument can be remotely programmed, exercised by external commands which are applied to a single 50-way socket on the rear panel.

7.5.2 To set the instrument to remote operation, depress the EXT PROG push-button. All front panel manual functions are now inhibited. Logic levels are as for standard Texas 7400 series TTL integrated circuits: Logic 1: +2.4V min to +5V max
Logic 0: 0 to +0.4 max, sink capability 10mA.

7.5.3 The socket pin connections, input codes and operative levels are listed below:
All pin nos. refer to SKT.1

(a) Generator AMPLITUDE Range Setting (1 of n code)

Logic State		Range		Pin No.
1	selects	100mV	on	A4
1	selects	1V	on	B4
1	selects	10V	on	C4

(b) Generator FREQUENCY Range Setting

FREQUENCY RANGE	Pin Nos. D7	A8	B8	C8
1	0	0	0	1
2	1	0	0	1
3	0	0	0	0
4	1	0	0	0
5	0	1	0	0
6	1	1	0	0

(c) Generator Frequency Setting

Hundreds Pin No.	Tens Pin No.	Units Pin No.	BCD Code
C7	C6	C5	8
B7	B6	B5	4
A7	A6	A5	2
D6	D5	D4	1

(d) Generator Amplitude Setting

Hundreds Pin No.	Tens Pin No.	Units Pin No.	BCD Code
D3	D2	D1	8
C3	C2	C1	4
B3	B2	B1	2
A3	A2	A1	1

(e) Integration Cycles Setting

Pin No. A9	D8	Range
0	0	1
0	1	10
1	0	100
1	1	1000

(f) *Harmonic Selection*

Harmonic Selected	Pin Nos. BCD Code	A10 8	D9 4	C9 2	B9 1
1		0	0	0	1
2		0	0	1	0
3		0	0	1	1
4		0	1	0	0
5		0	1	0	1
6		0	1	1	0
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1

(g) *MEASURE*

Pin No.	Operative level
B10	logic 1 to logic 0 transition

(h) *Display Mode Setting* 1 of n code

Mode	Pin Nos.
C	C12
P	D12
P/DB	A13

(j) *Correlator MEASUREMENT Range Selection* 1 of n code

MEASUREMENT Selector	Pin Nos.
Ratio	
1	B12
2	A12
3	D11
4	C11
Absolute	
100 V	B11
10 V	A11
1 V	D10
0.1 V	C10

SECTION 4

CIRCUIT DESCRIPTIONS

1. INTRODUCTION

1.1. This section provides a circuit description (both in logical and mathematical terms) of the p.c. boards contained in SM2001. It is recommended that the reader refers to the ***Theory of Operation*** in ***Section 2*** of this manual, for a general understanding of the system, before proceeding further.

1.2. In the following descriptions, component references apply to components on the circuit diagrams included in the back of this manual

2. GENERATOR SECTION

S.E.L. Interconnection Diagram: B32687

The generator section contains the following boards:

(a) Voltage Control (Generator) Board (A)
(b) Digital-To-Analogue Convertor (Generator) Board (B)
(c) Digital Oscillator (Generator) Board (C).

2.1. Voltage Control (Generator) Board (A)

S.E.L. Circuit Diagram No: B32669
S.E.L. Assy No : B31480

2.1.1. The voltage control generator board performs two functions:

(a) generates a reference voltage, controlled by the SET V control, for the Digital-to-Analogue (D/A) Converter Generator (board B).

(b) accepts and buffers the output from board B to provide a low impedance output at the front panel, generator terminals.

2.1.2. **Reference Voltage Generation:** This circuit is formed by the following sections:

(a) Input buffers TR1 and TR2, and isolating transformer T1

(b) 10 bit counter, formed by IC's 2, 3, 4/12 and 5/12

(c) 10 bit store, formed by IC's 4/9, 5/9, 6 and 7

(d) Digital-to-analogue convertor stages TR4 to TR13

(e) Product amplifier IC8

2.1.3. The sequence of operation is as follows. A reset pulse, generated in the voltage control board (D), is applied to the 10-bit counter via buffer stage TR1, isolating transformer T1 and gates IC1/12, 1/2 and 1/4. The information in the 10-bit counter is entered into the 10-bit store slightly before the reset pulse by TR3.

2.1.4. Clock pulses, also generated in the voltage control board, are then applied to the counter A I/P of IC2, via buffer stage TR2, isolating transformer T1 and gates IC1/10, 1/6. The counter counts the number of clock pulses applied, this being proportional to the settings of the UP:DOWN push-buttons, with SET V depressed.

2.1.5. A reset pulse is generated (when the clock pulse train stops) by the voltage control board (D) which, firstly, transfers (via TR3) the counted value into the 10-bit store (IC4/9, IC5/9, IC6 and 7) and secondly, resets the counter. A small delay occurs between the transfer and reset pulse caused by capacitor C3 and resistor R8.

2.1.6. The output lines from the store control switch-transistors TR4 to TR13 (inclusive). The store output code determines which transistors are switched-in; causing currents to flow in the associated resistors (R20 to R29). A summed voltage at the junction of these resistors is applied to the product amplifier circuit IC8. If all transistor switches are open, then the output reference voltage V_o (see fig. 4.1) from IC8 will be, by inspection, zero (neglecting amplifier input current).

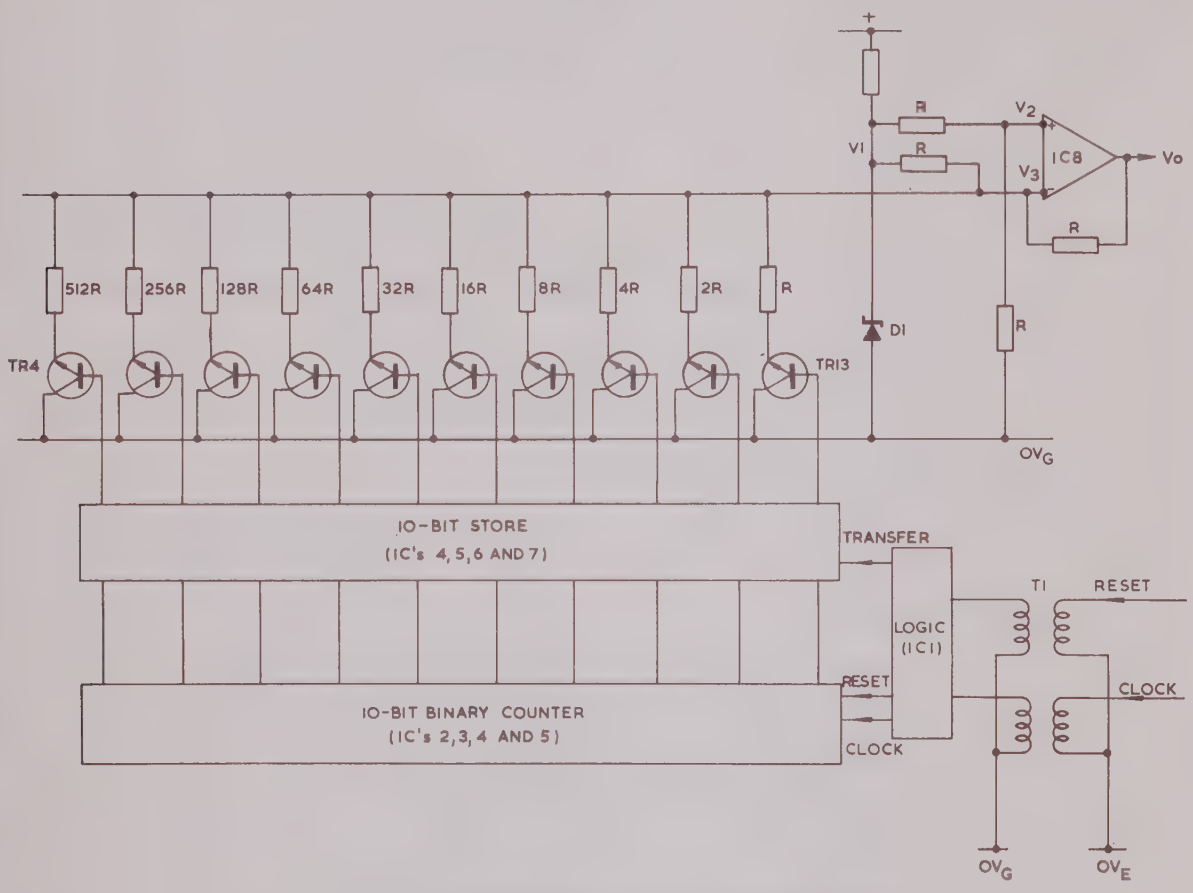


FIG. 4.1 REFERENCE VOLTAGE GENERATION

2.1.7. In general, the output voltage is calculated as follows:

$$V_2 = V_3 = \frac{V}{2} \qquad (V_2 \text{ is fixed for any number of switches closed}).$$

$$\therefore \quad \frac{V_1}{R} = \frac{V_1}{2R_s} - \frac{V_o - \frac{V}{2}}{R} \qquad \text{where } R_s = \text{switched resistance}$$

giving, $$V_o = \frac{V_1 R}{2R_s}$$

Thus, with switch S1 only closed, $$R_s = R$$

and, $$V_o = \frac{V_1}{2}$$

With Switch S2 only closed, $$R_s = 2R$$

and, $$V_o = \frac{V_1 R}{4R} = \frac{V_1}{4}$$

From this, it can be seen that with switch SW10 only, closed, $R_s = 512R$ and,

$$V_o = \frac{V_1 R}{512R} = \frac{V_1}{512}$$

2.1.8. **Output Amplifier** .. This is formed by transistors TR14 to TR20 inclusive. The analogue output from the digital-to-analogue convertor generator (board B) is applied as input to this amplifier.

2.1.9. Transistors TR14 and TR14′ form a differential amplifier with constant-current stage TR14″ in the tail. The stage is balanced by potentiometer RV2. Transistors TR15 and TR16 is a complementary pair (balanced by RV3) feeding another complementary pair TR19 and TR20. Current limiting of the output is provided by transistors TR17 and TR18 governing the amount of feedback applied to TR14′ base. The output is applied to the Hi and Lo generator output terminals.

2.2. Digital-to-Analogue Converter (Generator) Board (B)

S.E.L. Circuit Diagram No: E32670
S.E.L. Assy. No : B30706

2.2.1. The digital-to-analogue converter (generator) board converts the digital outputs from the digital oscillator generator (board C) into a sinewave, amplitude range controlled by 3 relays. These are controlled in turn, by the 3-position AMPLITUDE switch on the (generator section) front panel.

The board consists of 4 main sections:

(a) Input reference voltage buffer IC2 and associated circuitry.
(b) Digital-to-analogue conversion stages, TR1 to TR40 inclusive with weighting resistors R64 to R74 inclusive.
(c) Output buffer amplifier IC1 and quadrant switching stages TR41 to TR44.
(d) Relay switching circuits, TR47 to TR52 and relays RL1 to RL3.

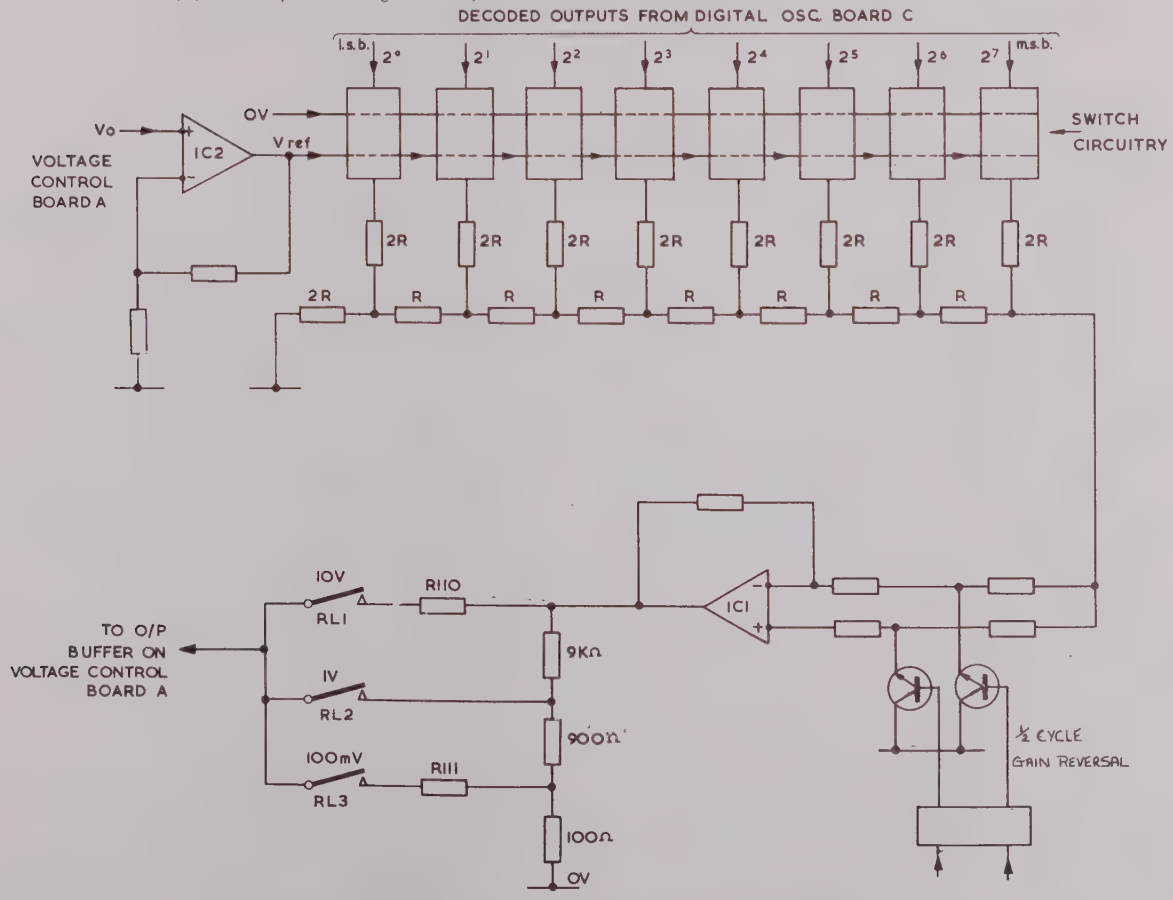


FIG. 4.2 BLOCK DIAGRAM OF THE DIGITAL-TO-ANALOGUE CONVERTER

2.2.3. The output from the voltage control board is referred to the Zener voltage (on that board) which has a tolerance spread around a nominal 9.1V. The reference voltage output at TR6 collector is about 10V, set up by RV5.

The sine and cosine, decoded, digital outputs 2^0 to 2^7 (inclusive) are alternately applied to D/A converters which follow the standard R-2R type converter principle. The converted levels are then applied to the output buffer amplifier IC1. The input pins (2 and 3) of IC1 are controlled by the quadrant switching stages TR41 to TR44.

2.2.4. A complete sinewave (at TP3) is achieved by:

(a) converting the sine register output (2^0 to 2^7) in the first quadrant (switch TR43 closed to 0V) then,

(b) converting the cosine register output (2^0 to 2^7) in the second quadrant (switch TR43 closed to 0V) then,

(c) converting the sine register output (2^0 to 2^7) in the third quadrant (switch TR44 closed, with IC1 inverting the input), then finally,

(d) converting the cosine register output (2^0 to 2^7) in the fourth quadrant (switch TR44 closed, with IC1 inverting the input).

2.2.5. Resistors R110 and R111 are fitted to present a constant source resistance to the output buffer amplifier for d.c. stability conditions.

2.2.6. The relay switching circuits are controlled by the AMPLITUDE switch. The relationship between switch position and relay energised is shown below:

AMPLITUDE posn.	Relay Energised
10V	RL1
1V	RL2
100mV	RL3

2.3. Digital Oscillator (Generator) Board (C)

S.E.L. Circuit Diagram No : B32671
S.E.L. Assy. No : B30920

2.3.1. The digital oscillator is the basic source of the generator section and provides sine and cosine decoded, digital information and quadrant information for conversion into a sine wave *(see also Section 2, Para. 3.2.5.).*

2.3.2. The digital oscillator is formed by cross-connecting two integrators (pulse counters) via multipliers. A pulse counter can be considered as an integrator as explained below:

If there is an input of X pulses in T seconds, then the counter contents will be X, assuming no overflow. This can be written as:

$$X = \int_0^T dt$$

Where dt is the input. This is the same, mathematically, as having X unit impulses, integrated in time T.

2.3.3. The frequency of the oscillator is determined by the input pulse rate (clock $\propto$ F input) which in turn, is set by the frequency and frequency range UP:DOWN push-buttons on the front panel of the instrument.

2.3.4. The digital oscillator is formed by cross connecting two integrators, via multipliers as shown below.

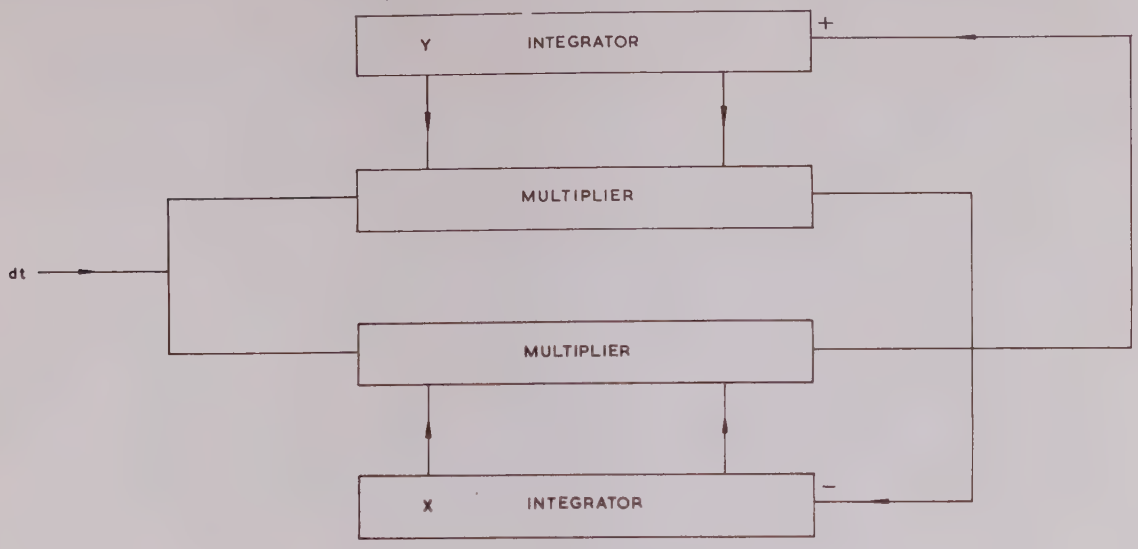


FIG. 4.3 DIGITAL OSCILLATOR

2.3.5. The following mathematic proof assumes that the correct starting conditions are set-up. The output of multiplier 1 is ydt and the output of multiplier 2 is Xdt.

$$\therefore\ y = \int X dt \quad \ldots\ldots (1)$$

and $$X = -\int y dt \quad \ldots\ldots (2)$$

From (1) $$X = \frac{dy}{dt}$$

$$\therefore\ \frac{dy}{dt} = -\int y dt$$

In D operator notation, this becomes:

$$Dy = -\frac{1}{Dy}$$

thus $$D^2y + 1 = 0$$

The solution of this is :—

$y = A\ (\text{Sin}\ \omega t + \text{Cos}\ \omega t\ )$ indicating an oscillating function.

2.3.6. With this configuration, one quadrant operation only is possible (as negative values are not possible with logic and the sign of the counting is fixed). The generation of the sine wave is therefore achieved by:

(a) D/A conversion of the sine register in the first quadrant (on board B)

(b) D/A conversion of the cosine register in the second quadrant (on board B).

(c) D/A conversion of the sine register in the third quadrant and inversion of the output (on board B)

(d) D/A conversion of the cosine register in the fourth quadrant and inversion of the output (on board B)

2.3.7. The sync input is used only when reference synchroniser SM2002 is fitted, to synchronise the generator section oscillator to an external oscillator.

3. EARTHY SECTION

S.E.L. Interconnection Diagram
No : E32689

The earthy section contains the following boards:—

(a) Voltage Control Board (D)
(b) Frequency Control Board (E)
(c) Frequency Range Control Board (F)
(d) Crystal Oscillator and Decimal Rate Multiplier Board (G)
(e) Cycles of Integration Board (K)
(f) Harmonic Selection Board (L)
(g) Cosine Register Board (M)
(h) Sine Register Board (N)
(j) Polar Log Control Board (P)
(k) Amplitude and Correlator Range Control Board (R)
(m) Display Board

3.1. Voltage Control Board (D)

S.E.L. Circuit Diagram No : B32672
S.E.L. Assy. No : B30921

3.1.1. The voltage control board performs four functions:

(a) gates the voltage or frequency information through to the display board, when the SET V or SET F pushbutton is depressed

(b) buffers the externally applied voltage control lines and gates them with the internal control lines, selected by the EXT PROG push-button

(c) buffers the voltage control lines out to the 50-way rear panel socket (SKT1) after the gating process mentioned in (b) above

(d) generates a clock train and reset pulse to the voltage control generator (board A) and the voltage control correlator (board U).

The principle of operation is described in *Section 2, Para. 3.2.9'.*

3.2. Frequency Control Board (E)

S.E.L. Circuit Diagram No : E32673
S.E.L. Assy. No : B30922

NOTE: The following description is in addition to the principle of operation as described in *Section 2, Para. 3.2.7.*

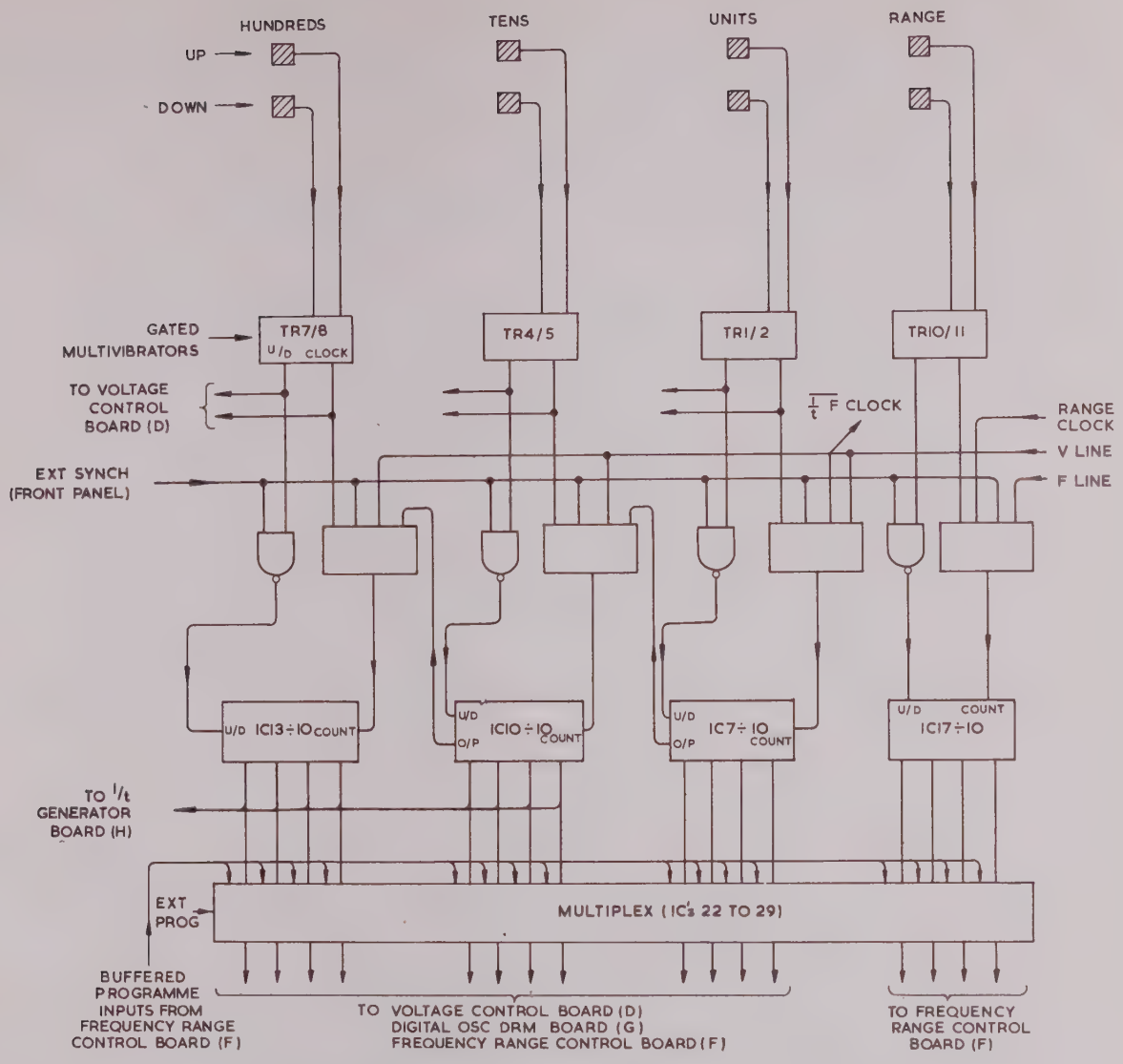


FIG. 4.4 FREQUENCY CONTROL LOGIC

3.2.1. Operation of either the UP or DOWN push-buttons enables the associated multivibrators (TR1 and 2, 4 and 5, 7 and 8, 10 and 11) to oscillate at 2Hz. At the end of each cycle, a narrow pulse is generated. This, together with the UP:DOWN information is gated into the frequency counters (IC's 7, 10, 13, 17) when the SET F push-button is depressed.

3.2.2. If the SET V push-button is depressed, this information is routed to control the voltage control counters on board D; in this state, the frequency counters on board E are inhibited.

3.2.3. If the EXT SYNC push-button is depressed (and Reference Synchroniser SM2002 is fitted), the count inputs from the front panel push-buttons are inhibited. The counters are connected in series and made to count down from 999, this value being set-in on the counter load inputs (pins 11) from the $^1/t$ generator board (H).

3.2.4. With the multivibrators oscillating at 2Hz, the maximum time to adjust each digit is 2.5 seconds (the counters overflow, so 0 to 9 and 9 to 0 are only one clock pulse).

3.2.5. The range counter (IC17) cannot overflow and is limited to the six ranges used. In the EXT SYNG mode, the range is set to 999Hz (unless harmonics are selected, when 99.9 Hz range is set) and ranges are changed down when 099 is detected (on $^1/t$ generator board H).

3.2.6. The outputs from the counters are fed to the multiplex gating logic (IC's 22 to 29 inclusive). This selects internal or external programme information to be passed on. The other input to the multiplexer is derived from the frequency range board (F), which contains the buffers for the external inputs.

The tens and hundreds frequency information is routed to the $^{1}/_{t}$ generator board H, to address the decimal rate multipliers.

3.2.7. The frequency control outputs (units, tens and hundreds) are routed to:

(a) crystal oscillator and DRM board (G), as addresses for the decimal rate multipliers

(b) frequency range control board (F) to be buffered before routing to the 50-way connectors on the rear panel

(c) voltage control board (D) to be multiplexed with the voltage control lines and displayed in the L.H. display, when the SET F push-button is depressed.

3.2.8. The frequency range control outputs are routed to the frequency range control board (F).

3.3. Frequency Range Control Board (F)

S.E.L. Circuit Diagram No: E32674
S.E.L. Assy. No: B30923

3.3.1. This board performs the following functions:

(a) it buffers the programme frequency and range inputs from the rear panel sockets and also buffers the frequency and range outputs to the rear panel sockets (gates IC1 to 12 inclusive)

(b) it uses the STOP push-buttons on the front panel to stop the generator output at any quadrant.

The divide-by-four counter (shown in fig. 4.5 below), comprises bistables A and B (IC's 2 4). This generates squarewaves, which, when gated, give the four quadrants uniquely when used in conjunction with the sync pulse from the digital oscillator generator board (C). When the 0^{0} STOP push-button is depressed, bistable C (IC27/13) is triggered at the next zero degree point of the waveform. The stop line is then energised to the rate inputs (clock $\propto$F and clock $\propto$10F) to the generator and correlator sections (see (d) below).

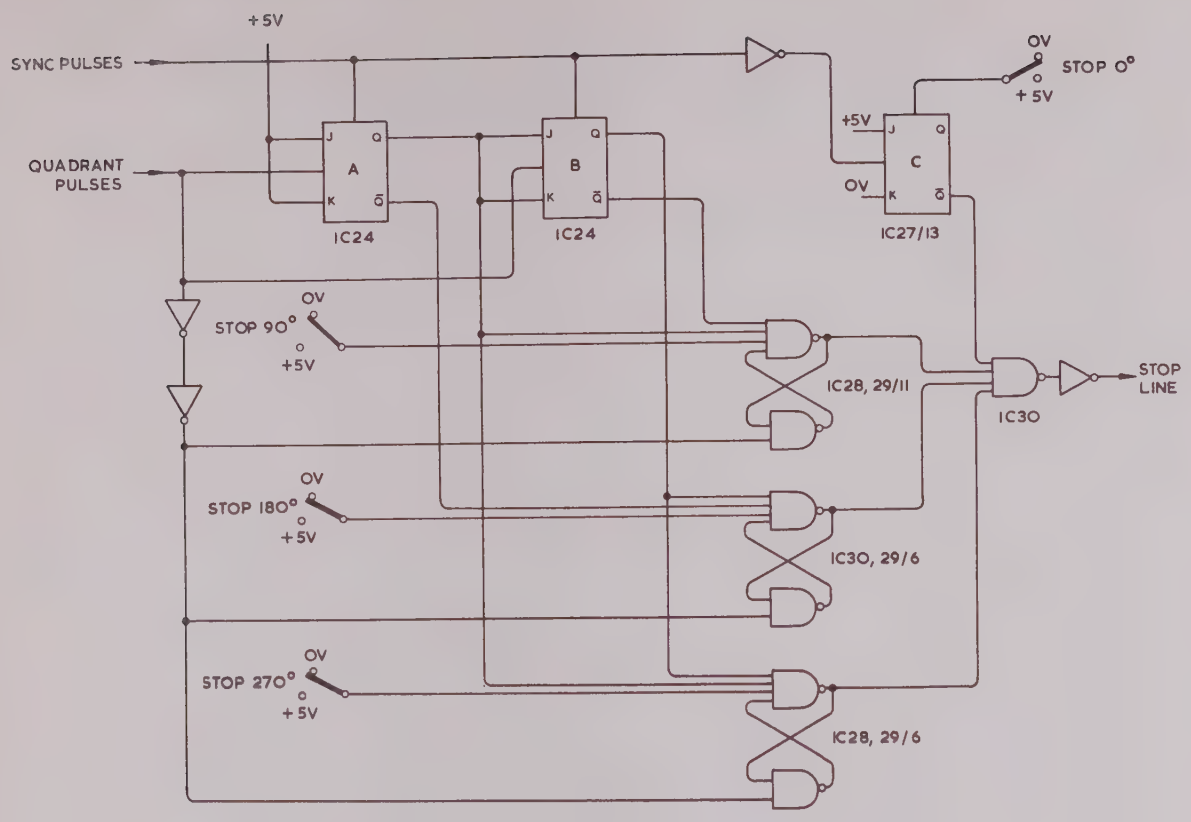


FIG. 4.5 QUADRANT STOP LOGIC

The 90°, 180° and 270° STOP circuits operate with a slight difference in that the gate bistables (IC's 28/29/6, 30/29, 28/29/8) are energised. When the selected quadrant point is reached, the energised gate bistable changes state and the rate signals to the generator and correlator sections are inhibited (see (d) below).

The ½-cycle output from the 'stop' logic is used in the Frequency Extension Unit SM2003 as the low-frequency locking signal.

(c) it uses the generator voltage and frequency range information to control the neons and decimal points of the L.H. display. The SET F and SET V push-buttons determine whether frequency or voltage units are displayed.

(d) it adjusts the rate output to the generator and correlator sections in decade steps, controlled by the FREQUENCY RANGE UP:DOWN push-buttons or by the external programme inputs. There are two outputs generated by dividers IC's 23, 26, 32, 33 and 39:

(i) clock $\propto$ F. This is always routed to the digital oscillator generator board (C).

(ii) clock $\propto$ 10F. This is used in the correlator section when harmonics 2 to 9 are selected, as the digital oscillator correlator (board S) runs at the harmonic frequency.

The decoded counter outputs are selected by decoding the frequency range information from BCD to 1-of-n, and using gates (IC's 22/3, 22/11, 31/3, 31/11,

35/11.and 37/8).

(e) the x1000 and sync inputs are used when the SM2001 is operated in conjunction with the Modulator-Demodulator SM2004.

3.4 Crystal Oscillator and DRM Board (G)

S.E.L. Circuit Diagram No :B32684
S.E.L. Assy. No : B30924

3.4.1. This board can be divided into two sections:

(a) .. crystal oscillator, set to 6.740 MHz

(b) three decimal rate multipliers (DRM).

3.4.2. The crystal oscillator is formed by crystal X1, transistors TR1 and TR2 and associated components. The 6.740MHz output is fed via gate IC33/8 to the decimal rate multipliers and also to the voltage control board (D) and the frequency range control board (F). A simplified circuit, with timing diagram, of a DRM is shown in fig. 4.6

3.4.3. Each DRM is basically the same, except that additional gating is required after the first DRM, because successive stages are operating at one-tenth and one-hundredth of the first DRM's speed. The various J K inputs follow the clock information as shown. The addresses to the DRM's are derived from the frequency control board (E) and originate either from the internal source or external (programme) source, selected by the EXT PROG push-button on the front panel.

3.5. System Description of Cartesian to Polar and Log Polar Conversion

3.5.1. The conversion is performed by the following interconnected boards:

(a) Cycles of integration board (K)
(b) Harmonic selection control board (L)
(c) Cosine register board (M)
(d) Sine register board (N)
(e) Polar log control board (P)

Derivation of Cartesian Values

3.5.2. In mathematical terms, the two product outputs from the correlator section are:

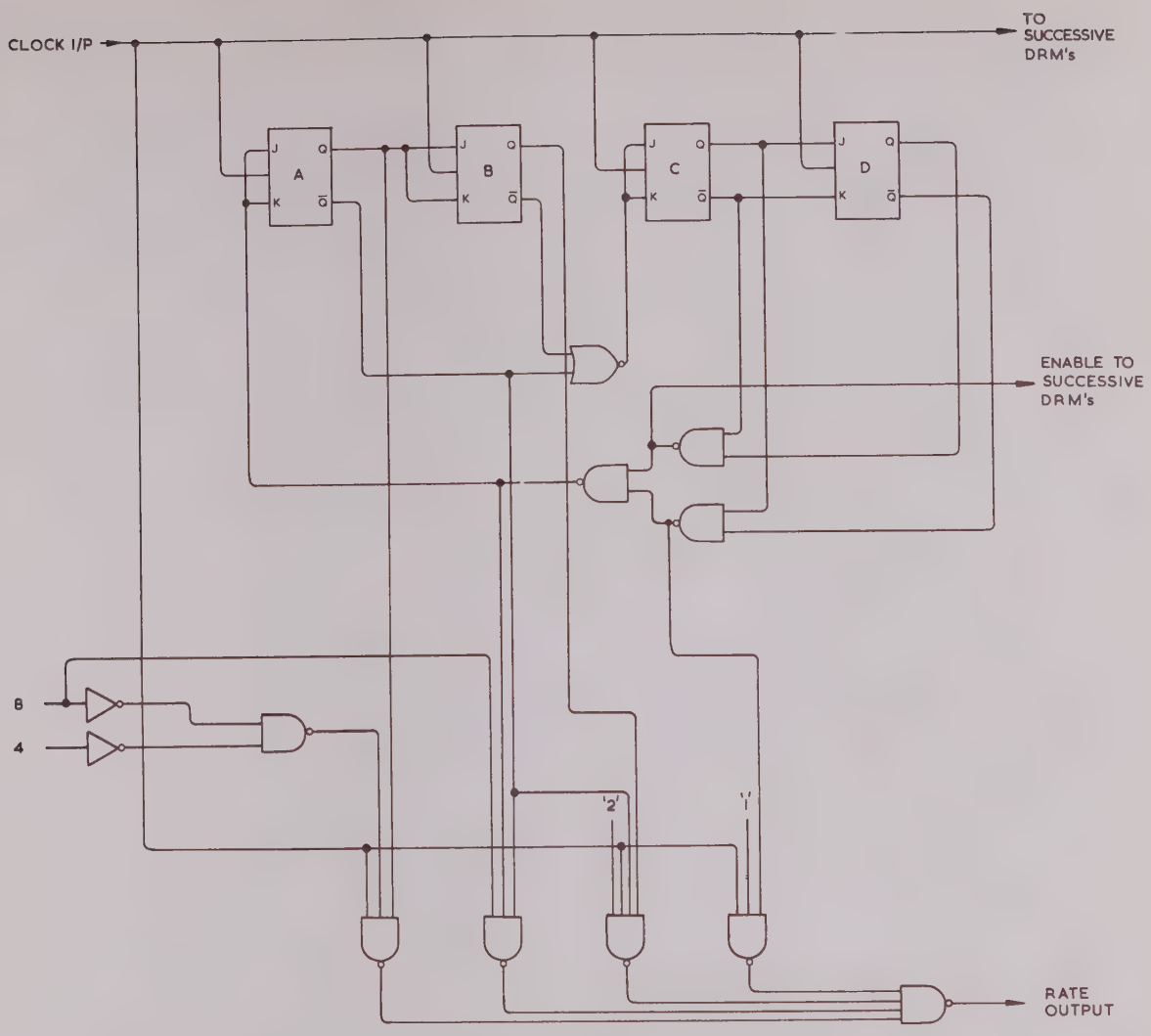
(1) ..... (a) Sin Product: $n\omega[A_1 \sin(\omega t + \phi_1) + A_2 \sin(2\omega t + \phi_2) \ldots\ldots \text{etc}] \sin n\omega t$

(2) ..... (b) Cos Product: $n\omega[A_1 \sin(\omega t + \phi_1) + A_2 \sin(2\omega t + \phi_2) \ldots\ldots \text{etc}] \cos n\omega t$

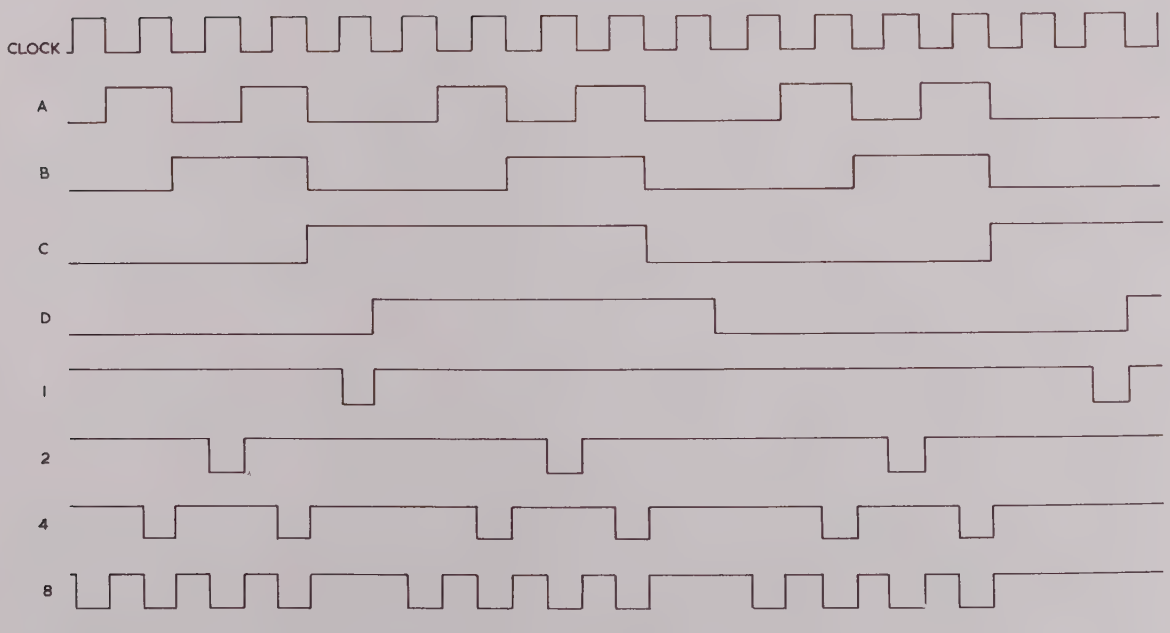
Where : $[A_1 \sin(\omega t + \phi_1) + A_2 \sin(2\omega t + \phi_2) \ldots\ldots \text{etc}]$ is the input signal, and $n\omega \sin n\omega t$ and $n\omega \cos n\omega t$ are the in-phase and quadrature components generated by correlator digital oscillator board (S).

If (1) and (2) are integrated over an integral number of pulses, M:-

$$I_1 = \int_0^{\frac{2M\pi}{\omega}} n\omega \sin n\omega t \,[A_1 \sin(\omega t + \phi_1) + A_2 \sin(2\omega t + \phi_2) \ldots\ldots \text{etc}]\, dt \quad \ldots\ldots\ldots\ldots \quad (1)$$



DRM LOGIC



TIMING DIAGRAM

FIG. 4.6 DECIMAL RATE MULTIPLIER

$= K A_n M n \cos \phi_n$ Where: A_n is the amplitude.

ϕ_n is the phase shift of the n^{th} harmonic.

K is a constant. All other product terms are zero.

$$I_2 = \int_0^{\frac{2M\pi}{\omega}} n\omega \cos n\omega t \ [A_1 \sin(\omega t + \phi_1) + A_2 \sin(2\omega t + \phi_2) \ldots\ldots\text{etc}] \ dt \quad \ldots\ldots\ldots\ldots (2)$$

$= K A_n M n \sin \phi_n$ Where: A_n is the amplitude.

ϕ_n is the phase shift of the n^{th} harmonic.

K is a constant. All other product terms are zero.

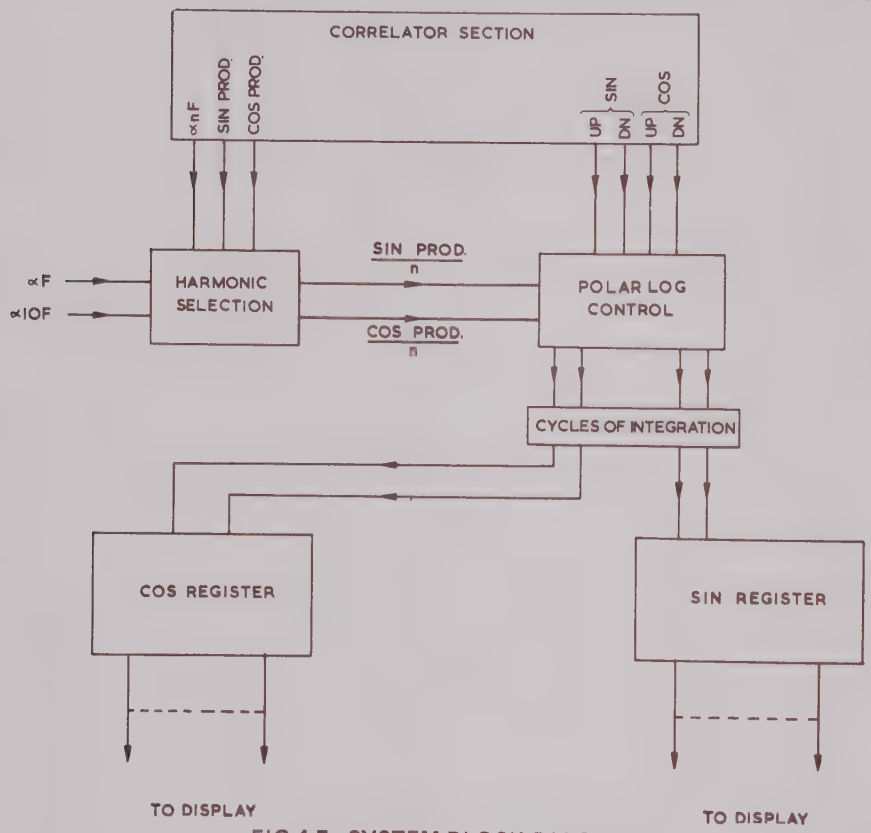


FIG 4.7 SYSTEM BLOCK DIAGRAM

3.5.3. The results required are $A_n \cos \phi_n$ and $A_n \sin \phi_n$. These are the cartesian values obtained by the measurement. The factor n is removed by the modulo n dividers in the harmonic selection control board (L). M is removed by the cycles of integration board (K) and the constant K is removed in the scaling.

3.5.4. The values, therefore, appearing at the cosine register and sine register are $A_n \cos \phi_n$ and $A_n \sin \phi_n$, respectively. This is the result displayed when the C (cartesian) push-button is depressed.

Conversion to Polar

3.5.5. When the P (polar) push-button is depressed, the displays are used to display A_n and ϕ_n by a conversion technique shown in simplified form on fig. 4.8.

3.5.6. The cosine register and sine register are interconnected via the rate multipliers to operate as a digital oscillator (as described in para. 2.3.2.). When the sine register reaches zero, the digital oscillator has moved round ϕ_n degrees and the cosine register contains the modulus $| A_n |$ of the input signal. At the same time as the dt pulses are driving the rate multipliers, they are also being fed into a store, the length of which is equal to the number of dt pulses required to rotate the oscillator through 90^o (the information relating to the relevant quadrant is derived from the $\pm$ sine and $\pm$ cosine lines on the display board.

3.5.7. When the sine register reaches zero, the rate multipliers are disconnected, and 900 is set into the sine register. Scaled pulses are then fed into the sine register. While the scaled pulses are being fed into the sine register, dt pulses are fed into the store until it is full. When this occurs, the scaled pulses are stopped and the sine register now displays the angle in 0.1^{O} increments. A count down from 900 is necessary because the store contains information relating to the complement,

$$-\left\{90 - \phi_n\right\} -, \text{ of the angle required.}$$

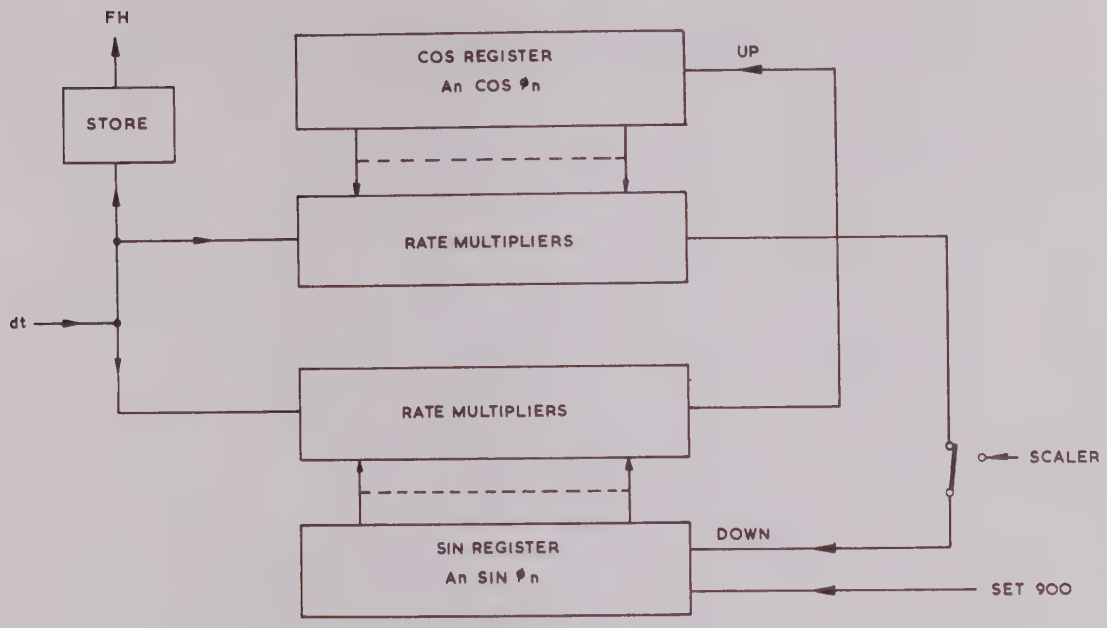


FIG. 4.8 POLAR CONVERSION

Conversion to Log Polar

3.5.8. When the P/dB (log polar) push-button is depressed, a further conversion takes place on the information in the cosine register

$(|\ A_n\ |)$ to produce the result,

(a) on ABSOLUTE ranges: $20 \log_{10} \dfrac{|\ A_n\ |}{10}$

(b) on RATIO ranges: $20 \log_{10} \dfrac{|\ A_n|}{V_o}$ where V_o is the generator output voltage.

The conversion is achieved as described on the next page (fig. 4.9).

3.5.9. When the register and multipliers are connected as shown, the value in the cosine register is:

$$Y = \int Y dt$$

the solution to this equation is:

$$Y = e^t$$

and $t = \log_e Y.$

This curve is followed until the cosine register overflows. When this occurs, the store is holding the equivalent of $\log_e T - \log_e A_n$, where T is the time taken to go from 1 to overflow in the cosine register. A starting dB value is then set into the cosine register, followed by a count in scaled pulses until the store is full, when the result displayed is the desired answer.

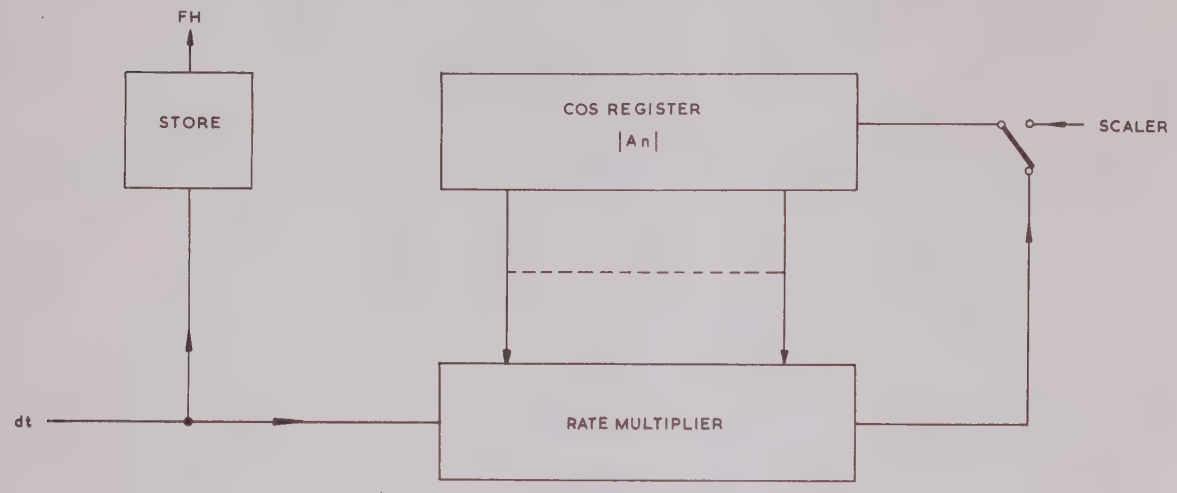


FIG. 4.9 LOG POLAR CONVERSION

3.5.10. The control circuits for the measurement and conversion are located on:

(a) cycles of integrated board (K) — measurement period, dividers.

(b) harmonic selection control board (L) — harmonic multiplication and division.

(c) polar log control board (P) — controls the up and down lines to the integrators, generates ± sine and ± cosine signals for the display board, selects which counting pulses are fed into each of the integrators, uses various lines from the other boards to sequence the various conversions.

3.6. Cycles of Integration Control Board (K)

S.E.L. Circuit Diagram No : E32746
S.E.L. Assy. No : B30925

3.6.1. Fig. 4.10 shows a simplified block schematic of this board. The board can be divided into four main sections:

(a) Integration time divider logic,
(b) Synchronous divider for cosine register,
(c) Synchronous divider for sine register,
(d) Internal/external gating logic.

3.6.2. A large amount of gating logic is required to interconnect the sine and cosine synchronous dividers on the board to the sine and cosine register boards, due to the type of synchronous integrated circuits used. The gating interconnects the various carry and enable lines between the stages which have to be altered for the different number of cycles of integration selected by the front panel selector.

3.6.3. The integration time divider logic uses the quadrant information from the generator section, digital oscillator board (C). Thus, integration is carried-out over 1, 10, 100 and 1000 cycles of the generator section output waveform.

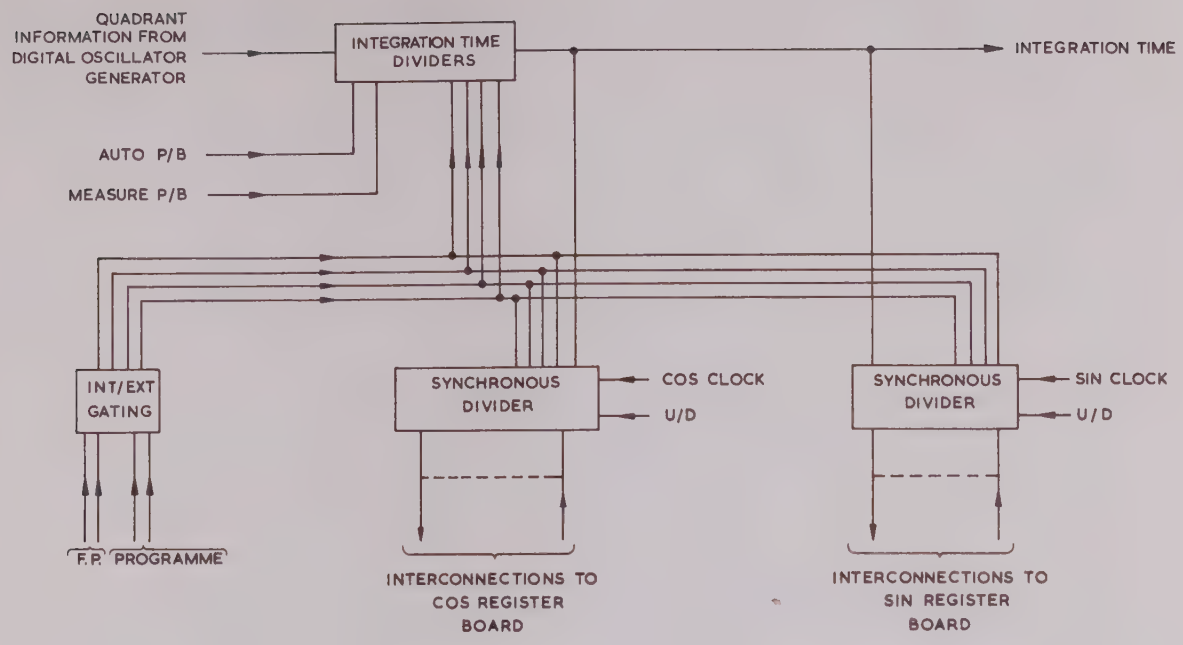


FIG. 4.10 GENERATION OF INTEGRATION TIME

3.6.4. The function of this board is described under *System Description — Cartesian to Polar and Log Polar Conversion.*

3.7. Harmonic Selection Control Board (L)

S.E.L. Circuit Diagram No : B32745
S.E.L. Assy. No : B30926

3.7.1. This board multiplies (up) the correlator digital oscillator frequency by increasing the number of pulses into the correlator section. It divides the sine and cosine products which are the output products of the correlator section *(see also System Description — Cartesian to Polar and Log Polar Conversion).*

3.7.2. The circuits on this board can be considered as five sections (see fig. 4.11):

(a) decimal rate multiplier, formed by four bistables IC2/IC8 and gates IC1 to IC7 (inclusive),

(b) modulo n divider logic, formed by the four bistables IC12 and 15, inverters IC11 and gates IC13 to 18/6 inclusive, for the sine product,

(c) modulo n divider logic, formed by the four bistables IC21 and 24, inverters IC20 and gates IC18/8, 22, 23 and 26, for the cosine product,

(d) internal/external gating logic for the harmonic selection information, either from an external programme source, or the front panel HARMONIC selector. The gating logic is formed by the adder IC27 and associated gate IC's 9/8, 19 and 28 to 32 inclusive.

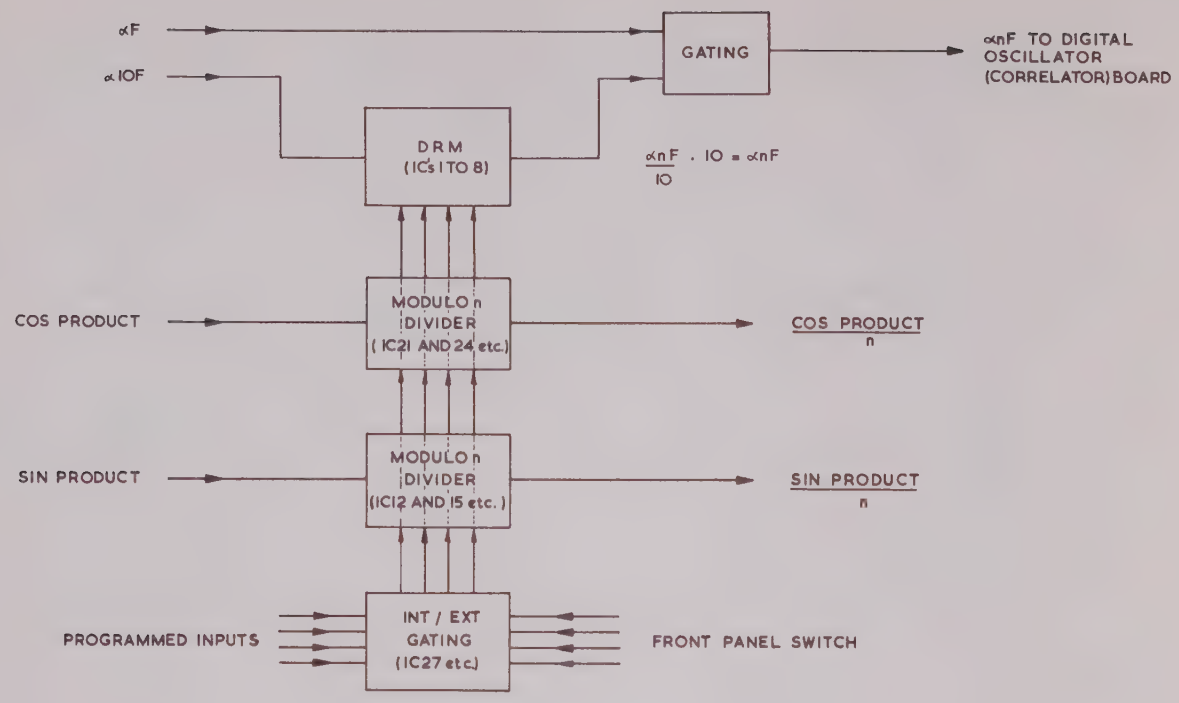

∝F
∝ IOF
GATING
∝nF TO DIGITAL OSCILLATOR (CORRELATOR) BOARD
DRM (ICs 1 TO 8)
∝nF / IO . IO = ∝nF
COS PRODUCT
MODULO n DIVIDER (IC2I AND 24 etc.)
COS PRODUCT / n
SIN PRODUCT
MODULO n DIVIDER (IC12 AND 15 etc.)
SIN PRODUCT / n
PROGRAMMED INPUTS
INT / EXT GATING (IC27 etc.)
FRONT PANEL SWITCH

FIG. 4.11 HARMONIC SELECTION LOGIC

3.8. Cosine Register Board (M) and Sine Register Board (N)

Board M – S.E.L. Circuit Diagram No : B32675
– S.E.L. Assy. No : B30927
Board N – S.E.L. Circuit Diagram No: B32676
– S.E.L. Assy. No : B30928

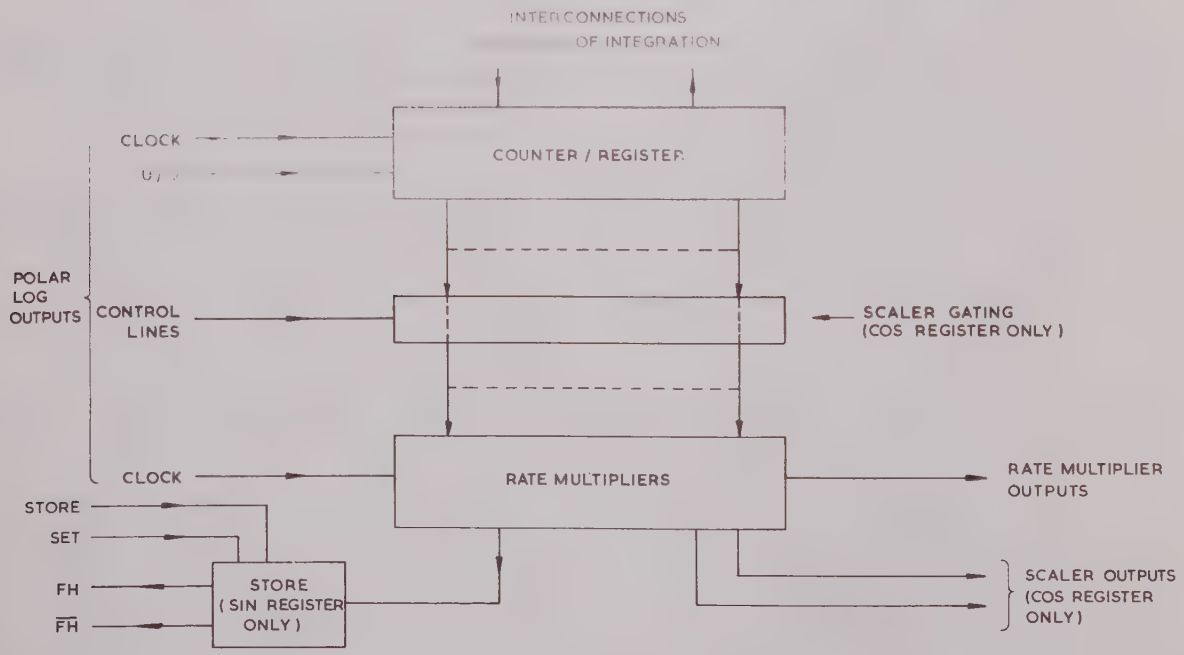


FIG. 4.12 COSINE (OR SINE) REGISTER BLOCK DIAGRAM

3.8.1. These boards are similar, but the sine register board also contains a store; the function of this store and all other sections of these boards, are described under ***System Description — Cartesian to Polar and Log Polar Conversion.*** The cosine register board also contains the scaler gating logic for the polar log control line outputs.

3.9. Polar Log Control Board (P)

S.E.L. Circuit Diagram No: E32743
S.E.L. Assy. No: B30929

3.9.1. The board can be divided into five main sections:

(a) cosine register control section,
(b) sine register control section,
(c) sequence control section,
(d) divide-by-eight section,
(e) blanking control section.

Cosine Register Control Section

3.9.2. A simplified diagram of this section is shown in Fig. 4.13. The reason for the complex gating to obtain the UP/DOWN lines, is shown in the table below. This shows that to increase a negative polarity means counting down (becoming more positive).

Polarity	Input Control	Output Control
+	UP	UP
+	DOWN	DOWN
–	UP	DOWN
–	DOWN	UP

3.9.3. It is also required that the UP:DOWN lines cannot be altered while the counter is being clocked. This means that only half of the gates' input pulses are counted into the register, the other half being used to control the UP:DOWN lines.

3.9.4. The A, B, C and D inputs function as follows. The A input inhibits the UP:DOWN lines during the conversion period only. The UP and DOWN signals are continously present whether a measurement is being taken or not. If these signals were allowed through while conversions were being made, they would upset the UP:DOWN lines and prevent a correct conversion being made. The B and C inputs are synchronous UP and DOWN signals used during the polar log conversion. The D input is an asychronous, overriding, UP control signal used during the polar conversion.

3.9.5. During a measurement, the A, B, C and D signals are high and have no affect on the measurement, so that the $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$ signals are passed through to gates IC3/6 and IC3/12. These are cross-coupled to form a gate bistable. The $\overline{\text{UP}}$ and $\overline{\text{DOWN}}$ signals cannot occur simultaneously.

3.9.6. The outputs of IC3/6 and IC3/12 are fed to bistable IC2/9 which changes state to follow IC3/6 and 3/2 on the next pulse derived from the product input. The outputs of IC3/6 and 3/2 are also gated into NOR gates IC5/4, 5/1 when the cosine register equals zero. These gates are also cross-coupled to form a bistable.

3.9.7. The outputs of gates IC23/11 and 23/8 are thus determined by bistable IC2/9 and gates IC5/4 and 5/1. The UP:DOWN requirement shown in the aforementioned table is derived from these outputs.

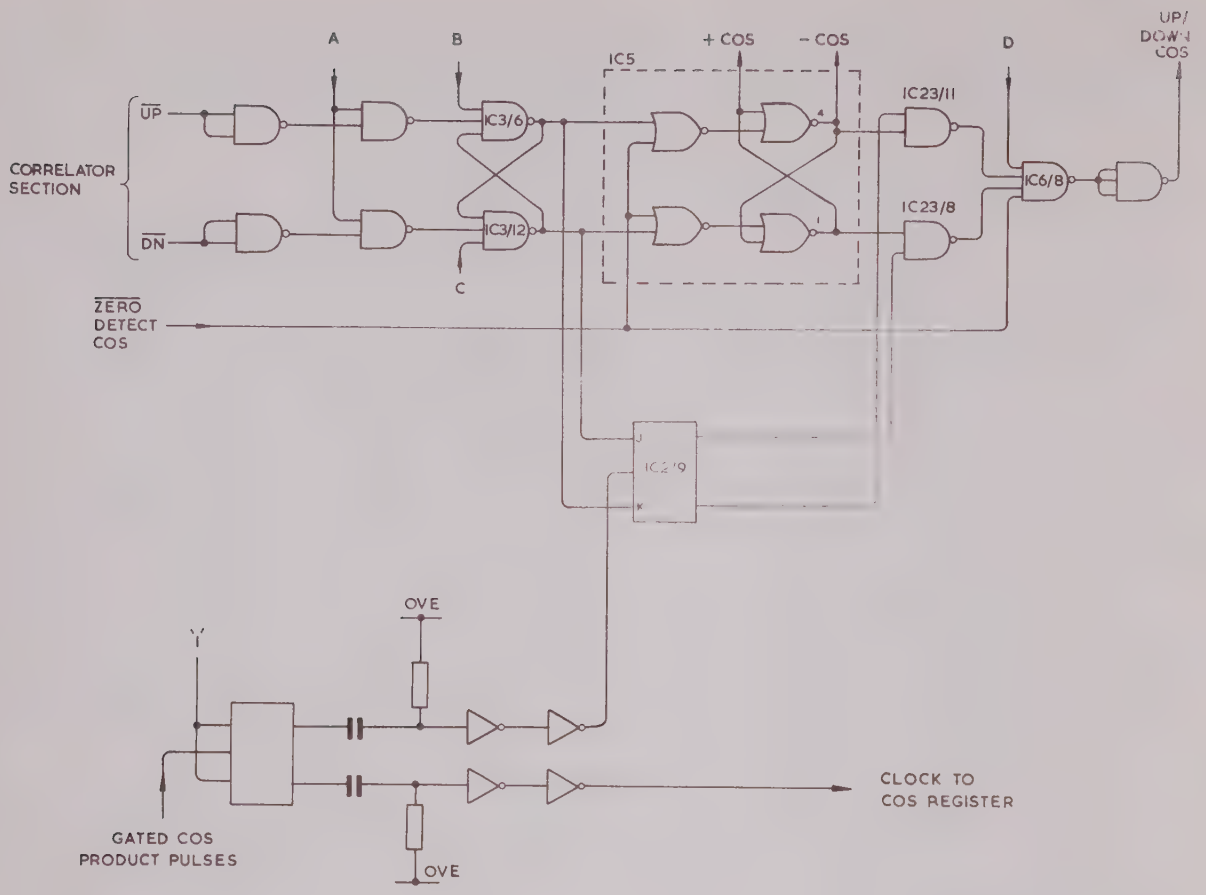


FIG. 4.13 COSINE REGISTER CONTROL

3.9.8. IC6/8 uses this information and the $\overline{\text{ZERO}}$ detect input (this automatically causes the counter to count up at zero, the polarity being derived by gates IC5/4 and 5/1) to bring the information down to one line; the synchronous counter used in the registers only require one line.

Sine Register Control Section

3.9.9. This section operates on the same principle as the cosine register control section, but control lines A and D only are used and D is used to cause the sine register to count down.

Sequence Control Section

3.9.10. The heart of the sequence controller is shown in fig. 4.14. The outputs from the gates and bistables shown are used to generate the necessary control lines for the other sections of the board.

3.9.11. The bistables (IC's 12/9, 12/12 and 18/12) are reset by the Reset 2 input. A measurement period starts. Bistable IC12/9 is clocked on the trailing edge of the integration time input. If the C (cartesian) push-button is depressed, this is the end of the sequence as the displays will have the desired results.

3.9.12. When bistable 12/9 is clocked, the D line ($\overline{Q}$ output on the circuit diagram) goes to logic 0 and, asynchronously, puts the cosine register in the UP mode and the sine register in the DOWN mode. If the P (polar) or P/dB (log polar) push-button is depressed, and the sequence can proceed, the UP:DOWN lines are in the correct state.

3.9.13. The cosine and sine registers are cross-connected to form a digital oscillator (as discussed Para. 3.5.6.) until the sine register reaches zero and bistable 12/12 can change state; bistable 12/9 at logic 1, $\overline{C}$ at gate 14/12 at logic 1 and $\overline{\text{ZERO}}$ detect sine at gate 15/4, results in a logic 1 on the J input of bistable 12/12.

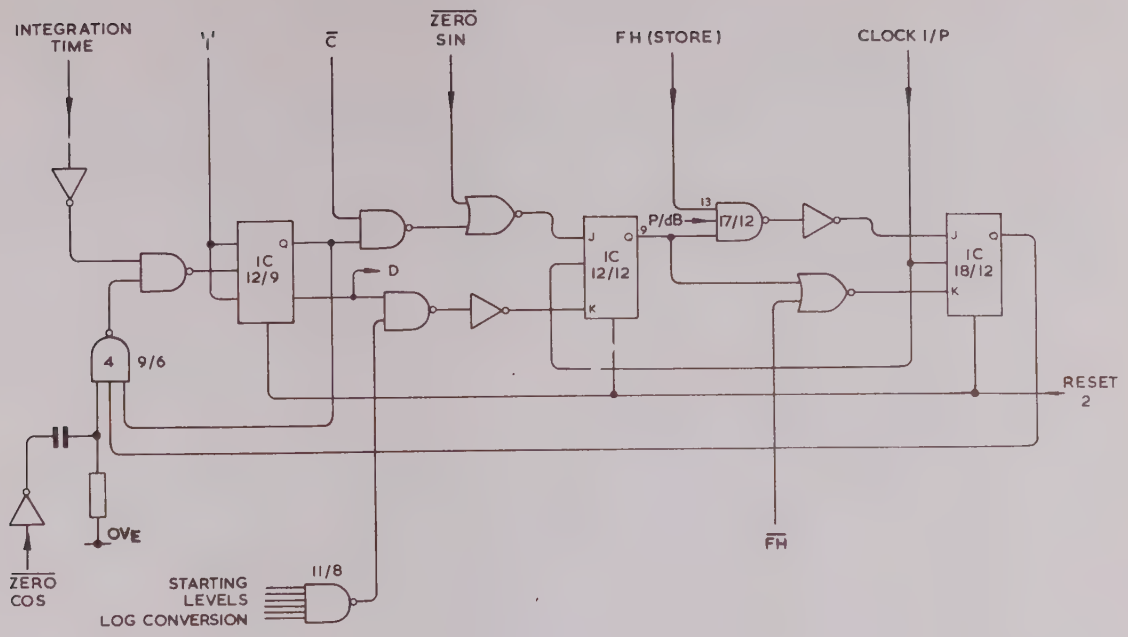


FIG. 4.14 SEQUENCE CONTROLLER

3.9.14. Bistable 12/12 changing state, changes the connections, so that no more pulses are fed into the cosine register, but scaled pulses enter the sine register to derive the angle.

3.9.15. When the store is full, the scaled pulses are inhibited so that no more are fed into the sine register. In the Polar mode, the sequence stops at this point, with the displays holding:-

$$|A_n| \text{ and } \phi_n.$$

3.9.16. If the P/dB (log polar) push-button is depressed, bistable 18/12 is clocked; the FH input at gate 17/13 is at logic 1, bistable Q12/12 is at logic 1 and with P/dB depressed, gate 17/2 is at logic 1. This initiates the e^t function (Para. 3.5.9). Gate IC9/6 is now enabled by the Q outputs of bistables 12/9 and 18/12, so that when the cosine register overflows (e^t section completed) the $\overline{\text{zero}}$ line clocks bistable 12/9 again, to stop the e^t sequence.

3.9.17. The gating now feeds pulses into the cosine register (but not the store) until the correct starting levels are reached and detected by the multiple input gate IC11/8. When this point is reached, bistable 12/12 is clocked again and generates a sychronous UP command to the cosine register. This action also allows scaling pulses to reach the register, until the store is full and the sequence ends with a display reading of:-

$$A_n \text{ (in dB) and } \phi_n.$$

Divide-by-Eight Section

3.9.18. All gated inputs to the sine and cosine registers (except the product inputs) pass through divide-by-eight dividers, one for sine inputs and one for cosine inputs. These are formed by bistables IC 30/12, 31/12 and 32/12 for cosine inputs and bistables IC30/9, 31/9 and 32/9 for the sine inputs. This process improves the conversion accuracy of the polar and log polar conversions.

Synchronous Clock

3.9.19. Bistables 12/12, 18/12 and 2/12 are clocked (only if the J K input pins are in the correct state) by the synchronous clock. This is formed by bistable 18/9 feeding gates IC's 33/3, 33/6. The input to this

circuit is the 0.674 MHz clock train from the clock and DRM board (G).

Blanking Control Logic

3.9.20. A non-stored display is used in the SM 2001. Therefore, during the measurement and conversion period, the display is blanked, so that continuously changing counter values are not displayed. This function is performed by bistables IC37/12 and 37/9 and associated gate logic.

3.10. Amplitude and Correlator Range Control Board (R)

S.E.L. Circuit Diagram No: B32677
S.E.L. Assy. No: B31486

3.10.1. This board forms part of the earthy section and accepts:

(a) 3 lines from the generator AMPLITUDE switch. These, together with 3 external programme input lines from the rear panel socket SKT 1 are gated to produce two sets of output lines:

(i) one to the voltage control, relay switching circuits on the digital-to-analogue board (B) in the generator section,

(ii) one to the display board, where it is gated with the correlator range information (front panel switch or external programme inputs). This information is used to control the positioning of the decimal points and to assign the units to the displayed value,

(b) 8 lines from the correlator range switch (MEASUREMENT – Absolute and Ratio), which are gated with external programme lines from the rear panel socket SKT1 and routed to the display board (see (ii) above). The four absolute lines are gated together to form two output lines which are routed to the relay switching circuits on the voltage control correlator board (U).

Similarly, 8 lines are also gated together to produce 4 lines which are routed to the analogue-to-digital converter board (V). Here, they control the range relay switching of the input buffer stage.

3.11. Display Board

S.E.L. Circuit Diagram No: E32699
S.E.L. Assy. No: B30935/6

3.11.1. The display board can be considered as seven sections:

(a) generator frequency and voltage amplitude display board,

(b) correlator cosine and sine display board,

(c) 'assigned units' neon gates and transistors,

(d) decimal point positioning gates and transistors,

(e) correlator amplitude control, gating logic,

(f) buffer gates for the correlator sine and cosine printer outputs, and switch setting information of the AMPLITUDE and DISPLAY selectors,

(g) +5V power supply to the logic.

3.11.2. The generator display board is fed with twelve lines of BCD information from the voltage control board (D). This is either voltage amplitude or frequency information, dependent upon whether the SET V or

SET F push-buttons (respectively) are depressed.

3.11.3. The correlator cosine and sine display board is fed with 12 lines of BCD sine information, 12 lines of BCD cosine information, a common display blanking signal (from the polar log control board P), decimal point lines and two overrange lines (one for the sine display and one for the cosine display).

3.11.4. Each 'assigned unit' neon, on the front panel, is energised by a switching transistor, which in turn, is switched by a gate. All these gates are fed with range information from the AMPLITUDE and DISPLAY selectors.

4. CORRELATOR SECTION

S.E.L. Interconnection Diagram No: B32688

The correlator section consists of the following:

(a) digital oscillator (correlator) board (S),

(b) digital-to-analogue converter board (T),

(c) voltage control (correlator) board (U),

(d) analogue-to-digital converter board (V),

(e) 8-bit binary rate multiplier (cosine) board (W),

(f) 8-bit binary rate multiplier (sine) board (X).

4.1. Digital Oscillator (Correlator) Board (S).

S.E.L. Circuit Diagram No: B32744
S.E.L. Assy. No: B30930.

4.1.1. In order that the polar and log polar conversion sequences can take place, a sine and cosine product is required by the polar log control board (P). As described in mathematical terms in Sub-section 3.5, these products are derived by multiplying the input signal :

$$[A_1 \sin(\omega t + \phi_1) + A_2 \sin(2\omega t + \phi_2) \ldots\ldots \text{etc}]$$

by the in-phase (sine) and quadrature (cosine) components, $n\omega \sin n\omega t$ and $n\omega \cos n\omega t$ respectively.

4.1.2. The digital oscillator is formed by cross-connecting two integrators (pulse counters IC8/IC14 and IC5/IC13) via multipliers. The action is similar to that described from the digital oscillator (generator) board C in Sub-section 2.3.

4.1.3. The frequency of the oscillator is determined by the input pulse rate (clock $\propto$nF) which is derived from the harmonic selection control board (L). The oscillator is phase-locked to the digital oscillator in the generator section by the SYNC input.

4.1.4. The UP and DOWN, sine and cosine, control signals (for the sine and cosine register control sections on the polar log board P and the correlator 8-bit binary rate multiplers boards W and X) are generated on this board. As digital pulses are monopolar by nature, polarity information has to be generated and this is done by using the ½-cycle bistable.

4.2. Digital-to-Analogue Converter (Correlator) Board (T)

S.E.L. Circuit Diagram No: B32678
S.E.L. Assy. No: B30931

4.2.1. This board accepts the 8-line digital output from the analogue-to-digital converter board (V) and

converts it to an analogue value for application to the comparator stage in the analogue-to-digital converter board (V).

4.2.2. The converter circuit is a standard R-2R converter, optimised for speed. The output of the ladder network is fed out directly to the summing junction of the comparator on the analogue-to-digital converter board (V).

4.2.3. The resistors of the ladder network are switched between positive and negative references. These are generated by IC's 1 and 2 from the reference voltage generated in the voltage control correlator board (U).

4.3. Voltage Control (Correlator) Board (U).

S.E.L. Circuit Diagram No: B32679
S.E.L. Assy. No: B30932

4.3.1. The voltage control (correlator) board generates a reference voltage, controlled by the SET V control for the digital-to-analogue converter correlator board (T).

4.3.2. **Reference Voltage Generation.** This circuit is formed by the following sections:

(a) input buffers TR1 and TR2, and isolating transformer T1

(b) 10-bit counter, formed by IC's 2, 3, 4/12 and 5/12

(c) 10-bit store, formed by IC's 4/9, 5/9, 6 and 7

(d) digital-to-analogue convertor stages TR4 to TR13

(e) product amplifier IC8.

4.3.3. The sequence of operation is as follows. A reset pulse, generated in the voltage control board (D), is applied to the 10-bit counter via buffer stage TR1, isolating transformer T1 and gates IC1/12, 1/2 and 1/4. The 10-bit store is also cleared at this time by a 'transfer' pulse generated (from the reset pulse) by TR3.

4.3.4. Clock pulses, also generated in the voltage control board, are then applied to the counter A I/P of IC2, via buffer stage TR2, isolating transformer T1 and gates IC1/10, 1/6. The counter counts the number of clock pulses applied, this being proportional to the settings of the UP:DOWN push-buttons, with SET V depressed.

4.3.5. A reset pulse is generated (when the clock pulse train stops) by the voltage control board (D) which, firstly, transfers (via TR3) the counted value into the 10-bit store (IC4/9, IC5/9, IC6 and 7) and secondly, resets the counter. A small delay occurs between the transfer and reset pulse caused by capacitor C3 and resistor R8.

4.3.6. The output lines from the store control switch-transistors TR4 to TR13 (inclusive). The store output code determines which transistors are switched-in causing currents to flow in the associated resistors (R20 to R29). A summed voltage at the junction of these resistors is applied to the product amplifier circuit IC8. If all transistor switches are open, then the output reference voltage V_o (see fig. 4.15) from IC8 will be,by inspection, zero (neglecting amplifier input current).

4.3.7. In general, the output voltage is calculated as follows:

$$V_2 = V_3 = \frac{V}{2}$$

(V_2 is fixed for any number of switches closed).

$$\therefore \quad \frac{V_1}{R} = \frac{V_1}{2R_s} - \frac{V_o - \frac{V}{2}}{R}$$

where R_s = switched resistance

giving $$V_o = \frac{V_1 R}{2R_s}$$

Thus, with switch S1 only closed $$R_s = R$$

and $$V_o = \frac{V_1}{2}$$

With switch S2 only closed $$R_s = 2R$$

and $$V_o = \frac{V_1 R}{4R} = \frac{V_1}{4}$$

From this, it can be seen that with switch SW10 only, closed, $R_s = 512R$

and $$V_o = \frac{V_1 R}{512R} = \frac{V_1}{512}$$

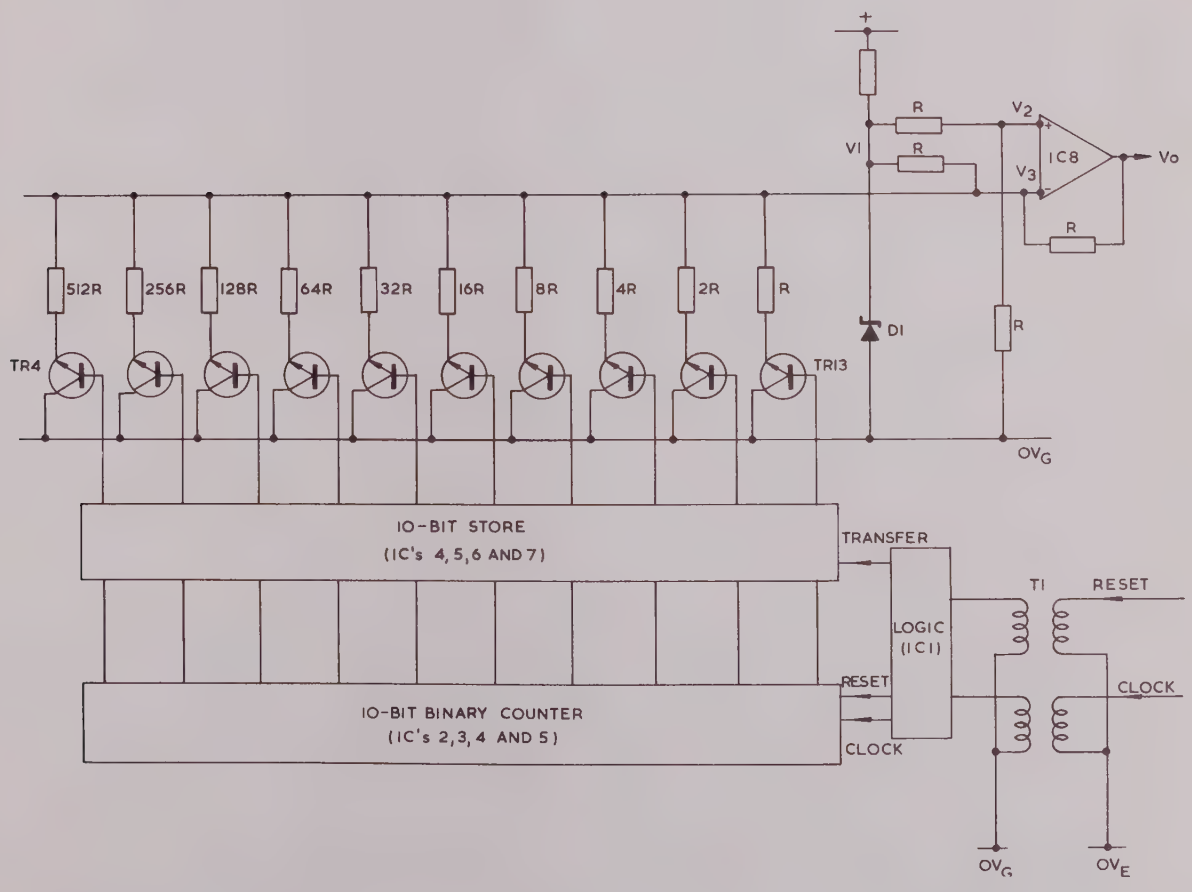


FIG. 4.15 REFERENCE VOLTAGE GENERATION

4.3.8. **Relay Switching Network.** Transistors TR15 and TR17 form this network which is controlled by inputs from the amplitude and correlator range board (R) in the earthy section.

4.3.9. Depending upon whether Ratio or Absolute measurements are being taken, so depends the output fed out to board T. This can be seen in the table below.

Measurement	Relay Energised	Output to Board T
Absolute	RL9	Zener reference from D1
Ratio	RL8	D/A output from IC8

4.3.10. Reed relays are used to isolate the earthy control signals from the floating correlator power supply.

4.4. Analogue-to-Digital Converter Board (V)

S.E.L. Circuit Diagram No: B32680
S.E.L. Assy. No: B30933

4.4.1. The purpose of this board is to convert the correlator input from an analogue waveform into digital information. The board consists of five main circuits:

(a) input buffer amplifier OA1, with range switching,

(b) comparator TR1 and IC16,

(c) 9-bit synchronous counter (IC5 and IC9), feeding IC's 10 and 13, each of which are quadruple 2 input exclusive OR gates,

(e) overload detect logic,

(f) range switching relay transistors.

A block diagram of the conversion logic is shown in fig 4.16 below.

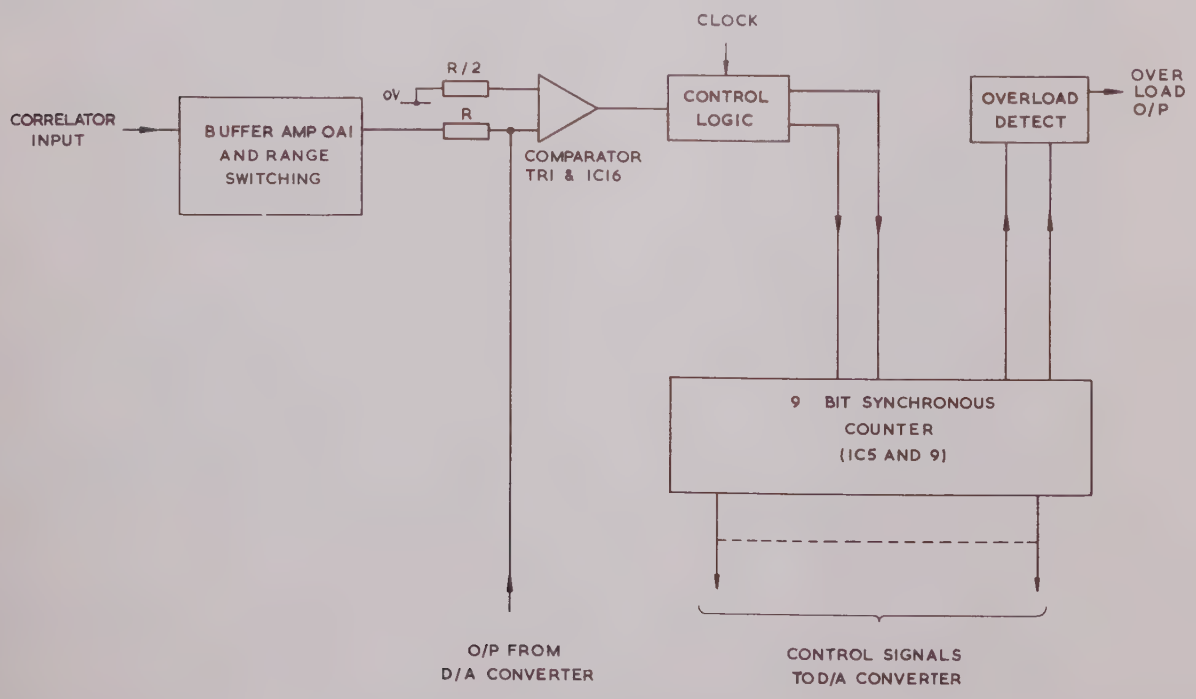


FIG. 4.16 A/D CONVERSION LOGIC

4.4.2. The correlator range control energises relays RL4 to RL7 (dependent upon switch position). The contacts of these relays are in the input buffer amplifier circuit and control the gain of amplifier OA1.

4.4.3. The step output of IC16 is inverted and the two outputs are applied to the control logic where they are gated by the CLOCK $\propto$ nF signal from the digital oscillator (correlator) board (S). The resultant clock train is applied to the inputs of both counters IC's 5 and 9. The system used only allows the counter to change on1least significant bit (l.s.b.) at a time, and this determines the maximum slewing rate of the conversion.

4.4.4. The most significant bits (m.s.b.) of the counter are used to generate the polarity decision. The remaining 8-bits are used by the sine and cosine binary rate multipliers (on boards W and X).

4.4.5. 8-bits have to be processed, so that for a positive polarity, the true outputs of the counter are applied to the binary rate multipliers. For a negative polarity, the not-true outputs (inverted) are used. This process is performed by the two quadruple exclusive-OR gate packages IC10 and IC18. A common output, taken from the polarity bistable IC2/12, is applied to all gates in these packages. The second input to each gate is a bit line from the counters. With a positive polarity, the most significant bit is at logic 1, and for a negative polarity it is at logic 0.

4.5. Binary Rate Multiplier Boards (W and X)

Board W — S.E.L. Circuit Diagram No: B32681
S.E.L. Assy. No: B31488
Board X — S.E.L. Circuit Diagram: B32691
S.E.L. Assy. No: B31488

4.5.1. There are two binary rate multiplier boards:

(a) board W is for cosine multiplication of the correlator input,

(b) board X is for sine multiplication of the correlator input.

4.5.2. Each board consists of two main circuits:

(a) binary rate multiplier (BRM) logic,

(b) BRM linearizing logic,

The outputs from these boards are:

$$A_n \sin (n\omega t + \phi_n)\, n\omega \sin n\omega t \quad \text{and,}$$

$$A_n \sin (n\omega t + \phi_n)\, n\omega \cos n\omega t$$

Where: A_n is the modulus of the amplitude of the n^{th} harmonic.

ϕ_n is the phase of the n^{th} harmonic.

4.5.3. **Rate Multiplier Principle.** The binary rate multiplier has two inputs: a pulse train of average rate input, R, and a parallel number input X. The output of the rate multiplier is a pulse train of average frequency equal to the product of its inputs.

$$O/P = R.X.2.^{-n}$$ where n is the number of divider stages.

4.5.4. On both p.c. boards (W and X), the counter section of the multiplier consists of eight synchronously clocked J-K master-slave bistables (IC's 2, 7, 11 and 16). The binary count sequence is controlled by the associated gating logic, with the rate input,

$$\overline{n\omega \sin n\omega t} \quad \text{or} \quad \overline{n\omega \cos n\omega t}$$

applied via gate IC1/8. The counter outputs are applied to a series of NAND gates, to which is also applied the BRM address code from the analogue-to-digital converter board (V).

4.5.5. The rate outputs of the counter are as shown below:

Bistable	No. of Pulses per 128 I/P Rate Pulses
16/9 (lowest rate O/P)	1
16/12	2
11/9	4
11/12	8
7/9	16
7/12	32
2/9	64
2/12 (highest rate O/P)	128

4.5.6. As the address code from the analogue-to-digital converter is also binary weighted, the most significant bit of the address is used for the highest rate from the multiplier and so on, down to the least significant bit addressing the lowest rate.

4.5.7. **BRM Linearizing Logic.** From the table above, it can be seen that the lowest rate output from the multiplier can only generate 1 output pulse for every 128 rate input pulses. It is essential, that in order to obtain a pulse output from each rate output line (from gates 22/6, 18/8, 15/3, 13/8, 10/6, 8/8, 6/6 and 4/8), a BRM address pulse must be present at the input to these gates, at the same time as the associated rate output pulse is applied from the counter section of the multiplier. In order to ensure that this is so, each bit of the BRM address is applied to a suitable number of divider decades before application to the multiplier. For example, the least significant bit of the BRM address is divided by 128 so that only the 128th pulse is applied to the lowest rate output gate (22/6).

4.5.8. From the table below, the amount of division required for each bit can be seen.

	BRM Address		BRM Rate Output
l.s.b.	128	Address lowest rate output	1
	64		2
	32		4
	16		8
	8		16
	4		32
	2		64
m.s.b.	1	Addresses highest rate output	128

5. POWER SUPPLY UNIT

5.1. Two types of unit have been designed for the SM2001:

(a) SM2001 instruments, serial suffix numbers /002 to / 006. Power units in these earlier instruments are fitted with adjustable d.c. supplies (S.E.L. circuit number: E32690).

(b) SM2001 instruments, serial suffix numbers /007 to /0025. Power units in these later instruments are fitted with non-adjustable d.c. supplies.

5.2. The power unit occupies the complete section across the rear of the instrument and is electrically divided into three main sections:

(a) generator supply

(b) earthy section supply

(c) correlator supply.

5.3. The mains input lines and d.c. output supply lines are connected to the distribution terminal blocks, TB1 and TB2, fitted along the top of the power unit. The primary windings of the three mains input transformers, T1, T2 and T3, are connected in parallel to each other and terminated on TB1, pins 1, 2, 3, and 4.

5.4. Mains Input Link Selection.

5.4.1. The connections of the transformers' primary windings can be varied to suit 115V or 230V inputs, by linking the individual windings of each transformer in series or parallel at terminal block TB1 (pins 1, 2, 3 and 4) as follows

Mains Operation	Link Pins on TB1
115V	2 to 3
230V	1 to 3, 2 to 4

5.4.2. Cooling Fan. It should be noted that the standard cooling fan is suitable for 115V or 230V mains inputs, but at frequencies of 50Hz to 60Hz only. For use on a mains frequency of 440Hz, the fan must be changed.

5.5. Power units, fitted to SM2001, serial suffix numbers /001 to /006.

5.5.1. The d.c. outputs from these supplies are as listed below.

(a) Generator (floating) supply

(i) stabilised $+5V_g$ (fixed)

(ii) stabilised $+17V_g$ (adjustable by preset RV2)

(iii) stabilised $-17V_g$ (adjustable by preset RV1)

(b) Earthy section supply

(i) stabilised $+5V_e$ (fixed)

(ii) stabilised $+17V_e$ (adjustable by preset RV4)

(iii) stabilised $-17V_e$ (adjustable by preset RV3)

(iv) unstabilised $+250V_e$ (fixed)

(c) Correlator (floating) supply

(i) stabilised $+5V_c$ (fixed)

(ii) stabilised $+17V_c$ (adjustable by preset RV6)

(iii) stabilised $-17V_c$ (adjustable by preset RV5)

5.5.2. **Separate OV Lines.** It should be noted that the OV lines on the d.c. output side of the three section supplies are isolated from each other, and these must never be interconnected. Throughout this manual and the instrument, these lines are assigned suffix letters as follows:

Supply	OV Line Suffix
Generator	OV_g
Earthy Section	OV_e
Correlator	OV_c

5.5.3. The +5V supplies incorporate output power transistors and are fused at values of:

Supply	Fuse
$+5V_g$	1A
$+5V_e$	5A
$+5V_c$	2.5A

Voltage stabilisation on all d.c. supplies (except $+250V_e$) is achieved by use of integrated circuit voltage regulators.

5.6. **Power Units for SM2001, serial suffix numbers /007 to /025**

5.6.1. This series of power unit does not incorporate preset potentiometers in the d.c. supplies. The unit is electrically divided into three sections, generating the following voltages:

(a) Generator supply

(i) stabilised $+5V_g$

(ii) stabilised $+18V_g$

(iii) stabilised $-18V_g$

(b) Earthy section supply

(i) stabilised $+5V_e$

(ii) stabilised $+18V_e$

(iii) stabilised $-18V_e$

(iv) unstabilsed +240V_e

(c) Correlator supply

(i) stabilised +5V_c

(ii) stabilised +18V_c

(iii) stabilised −18V_c

5.6.2. It is emphasized that the OV lines on the d.c. output side of the three section supplies are isolated from each other and these must never be interconnected. Throughout this manual and the instrument, these lines are assigned suffix letters as follows:

Supply	OV line suffix
Generator	OV_g
Earthy section	OV_e
Correlator	OV_c

SECTION 5

MAINTENANCE

1. INTRODUCTION

1.1. This section contains notes on preventive maintenance, an in-cabinet functional check and internal adjustment procedures.

2. PREVENTIVE MAINTENANCE

2.1. Instrument Cover Removal

2.1.1. To remove the top cover, loosen and remove the six cover retaining screws from the top of the instrument.

WARNING

115V or 230V a.c. and d.c. supply wires are exposed when the cover is removed.

2.2. Cleaning

2.2.1 The instrument should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation.

2.2.2. Thoroughly clean both the inside and outside of the instrument. Remove dust from inaccessible areas with low pressure compressed air or vacuum cleaner. Use alcohol applied with a cleaning brush to remove accumulations of dirt or grease from connector contacts and component terminals. Clean the exterior of the instrument and the front panel with a mild detergent mixed with water, applying the solution with a soft, lint-free cloth.

2.3. Visual Inspection

2.3.1. The instrument should be inspected occasionally for such defects as broken connections, loose, broken or frayed wiring, dirty or pitted switch and connector contacts and cracked or broken printed circuit boards. Often, before a total or partial failure occurs, a deteriorating component can be located due to obvious discoloration, cracking or warping. Care must be taken if heat-damaged parts are located. Over-heating is usually only a sympton of trouble. For this reason, it is essential to determine the actual cause of over-heating before the heat-damaged part is renewed, otherwise, the damage may be repeated.

2.4. Repair and Renewal of Parts

2.4.1. Repair and replacement of electrical and mechanical parts must be accomplished with caution. Printed circuit component boards can become warped, cracked or burnt from excessive heat or mechanical stress. The following repair techniques are suggested to avoid inadvertant destruction or degradation of parts and assemblies.

2.4.2 Use ordinary 60/40 solder and a 35 to 40-watt pencil type soldering iron on the circuit board. The tip of the iron should be clean and properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the circuit from the base material. To desolder components use a commercial "solder sipper".

Always replace a component with its exact duplicate as specified in the parts list.

3. IN-CABINET CHECKS

3.1. The procedure outlined in the following paragraphs can be used to verify the operation of the SM2001. It can be used:

(a) as part of the incoming inspection check,
(b) periodically, for instruments used in systems,
(c) after repairs or adjustments, before returning the instrument to regular service

For the following checks, it is not necessary to remove the top cover.

3.2. Cycles of Integration Check

(a) Connect the GENERATOR OUTPUT terminals to the CORRELATOR INPUT terminals (HIGH to HIGH, LOW to LOW).

(b) Set the front panel controls to the positions listed in the table below and check that the time taken for a display to appear is always 1 second.

Generator Voltage	Generator Frequency (Hz)	Cycles of Integration	Display Reading	Display Time Delay (seconds)
9.99V	1	1	9.99	1
9.99V	10	10	9.99	1
9.99V	100	100	9.99	1
9.99V	999	1000	9.99	1

(c) Check that the centre display reads correctly as shown.

3.3. Harmonic Selection Check

(a) Set the generator frequency to 9.99Hz. Set the generator output voltage to 9.99V. Select 10 cycles of integration. Set the MEASUREMENT selector to the ABSOLUTE IV range. The OVERLOAD indicator should light-up; for the purposes of this test it can be ignored.

(b) Check the displayed results against the following table in relation to the position of the HARMONIC selector. To obtain a new reading at each position, the MEASURE push-button must be depressed.

HARMONIC Selector Posn.	Centre Display (V)	R.H. Display (V)
1	+0.280	–0.596
2	0.000	0.000
3	+0.655	–0.004
4	0.000	0.000
5	+0.363	–0.003
6	0.000	0.000
7	+0.230	–0.003
8	0.000	0.000
9	+0.150	–0.003

(c) Disconnect the generator output from the correlator input.

NOTE: This is an operational test only and all readings are very approximate.

3.4. Phase Checks (fig. 5.2)

(a) Set the generator output voltage to 9.99V and the frequency to 72Hz (approx.). Connect the R-C network (shown in fig. A) across the GENERATOR OUTPUT terminals and connect the output of the network to the CORRELATOR INPUT terminals. Depress the RUN push-button.

(b) Set the correlator displays to Cartesian mode. Adjust the generator output voltage and frequency until (by repeatedly depressing the MEASURE push-button) both the centre and R.H. displays read 5.00.

(c) Set the correlator displays to Polar mode. Check that the centre display reads 7.07 and the R.H. display reads $45^{o} \pm 0.2^{o}$. Check that the quadrant display illuminates the bottom R.H. quadrant.

(d) Set the correlator displays to the Log Polar mode. Check that the centre display reads -3 dB $\pm$ 0.1 dB and the R.H. display reads $45^{o} \pm 0.2^{o}$.

(e) Connect the R.C. network in the configurations shown in fig. B, C and D in turn. Check that the centre display and R.H. display reads to the same values and tolerances in steps (b), (c), and (d) above for each setting of CARTESIAN, POLAR and LOG POLAR. Check that the quadrant changes to the position indicated in figs. B, C and D.

(f) Disconnect the phase networks.

3.5. 50Hz Effect

(a) Set the generator output voltage to 9.99V and the frequency to 50Hz. Select the cartesian display mode and 100 cycles of integration. Set the correlator MEASUREMENT selector to the ABSOLUTE 10V range. Depress the RUN push-button.

(b) Trigger the test oscilloscope from the 50Hz mains supply and monitor the output of the generator.

(c) Adjust the generator output frequency until it is synchronous with the mains supply frequency (the oscilloscope display becomes stable).

(d) Increase the generator output frequency by 0.2Hz from the setting in (c) above. Connect the generator output terminals to the correlator input terminals.

(e) Check that when the MEASURE push-button is repeatedly depressed, the maximum deviation from the generator output is not greater than ± 3 bits.

(f) Disconnect the generator output terminals from the correlator input terminals.

3.6. Output Impedance Check

(a) Set the generator output voltage to 9.99V and the frequency to 50Hz. Select cartesian display mode and 100 cycles of integration. Set the correlator MEASUREMENT selector to the ABSOLUTE 10V range. Depress the STOP 90^{o} push-button.

(b) Connect the test digital voltmeter to the GENERATOR OUTPUT terminals and note the indicated voltage. Call this V1.

(c) Connect a 250Ω ($\pm$5%) resistor across the HIGH and LOW GENERATOR OUTPUT terminals. Note the voltage indicated by the digital voltmeter. Call this voltage V2.

(d) Calculate the output impedance to be $< 1\,\Omega$ by use of the formula below:

$$\frac{V1 - V2}{V2} \times 250$$

4. INTERNAL CHECKS AND ADJUSTMENTS – SM2001

4.1. Identification of P.C. Boards

4.1.1. Each plug-in p.c. board is identified

(a) by a number etched onto the copper side of the board or,

(b) by an 'assembly' number, on those boards fitted with a board ident strip

(c) by the board's position in the instrument. Each board is plugged into an edge connector, and these are arranged alphabetically left to right across the instrument, starting with SKT A. The boards can also be identified by reference to fig. 5.1.

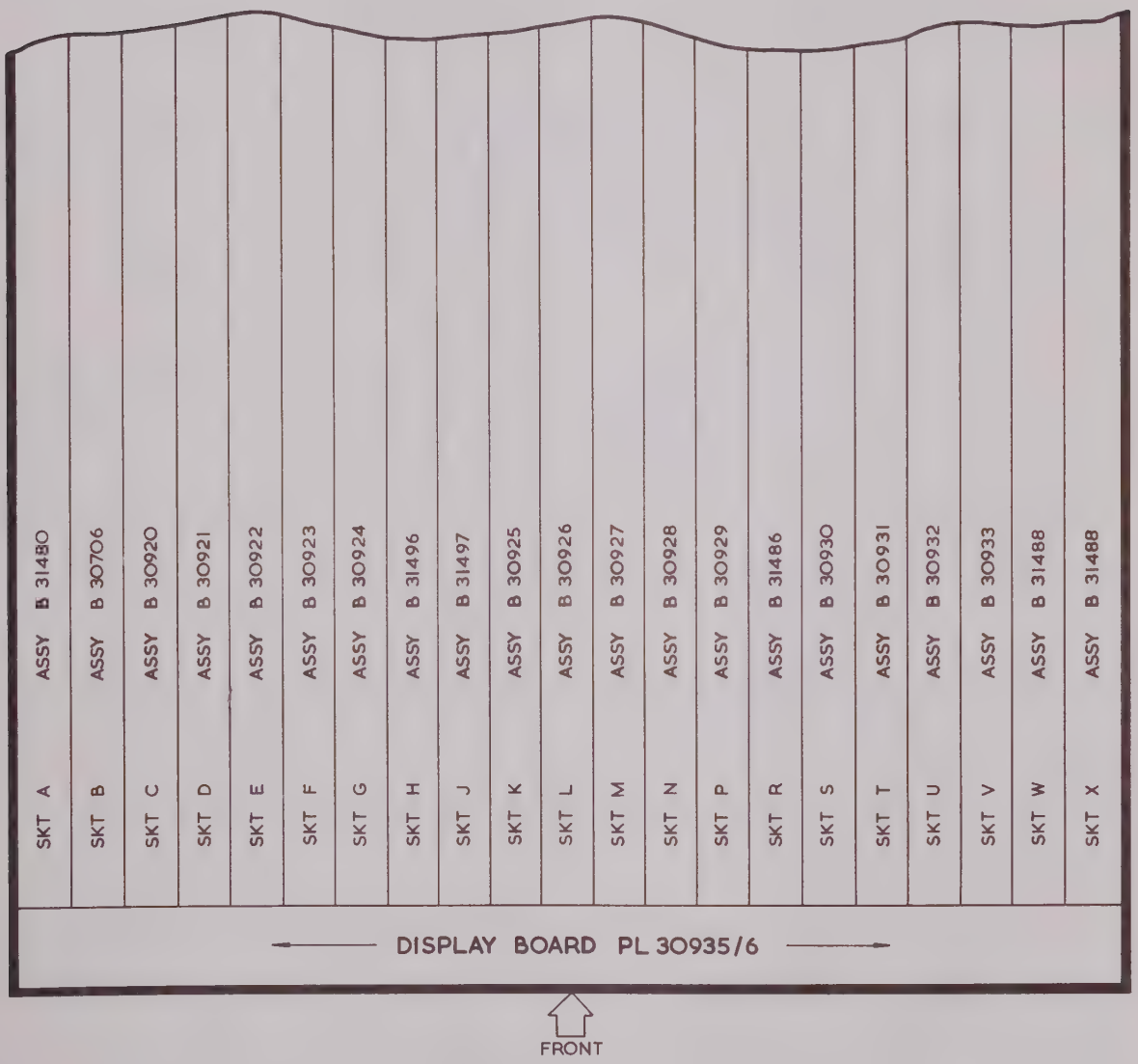

SKT A ASSY B 31480
SKT B ASSY B 30706
SKT C ASSY B 30920
SKT D ASSY B 30921
SKT E ASSY B 30922
SKT F ASSY B 30923
SKT G ASSY B 30924
SKT H ASSY B 31496
SKT J ASSY B 31497
SKT K ASSY B 30925
SKT L ASSY B 30926
SKT M ASSY B 30927
SKT N ASSY B 30928
SKT P ASSY B 30929
SKT R ASSY B 31486
SKT S ASSY B 30930
SKT T ASSY B 30931
SKT U ASSY B 30932
SKT V ASSY B 30933
SKT W ASSY B 31488
SKT X ASSY B 31488
DISPLAY BOARD PL 30935/6
FRONT

FIG. 5.1 IDENTIFICATION OF P.C. BOARDS

4.2. Test Equipment Required

(a) Timer/counter or frequency meter capable of measurement up to 7 MHz (S.E. Laboratories SM201 or SM202 or similar).

(b) Oscilloscope (S.E. Laboratories SM113 or similar).

(c) Sinewave generator range 1 Hz to 2 MHz, 2V p.p.

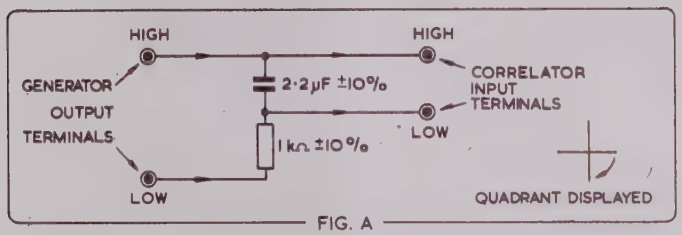


FIG. A

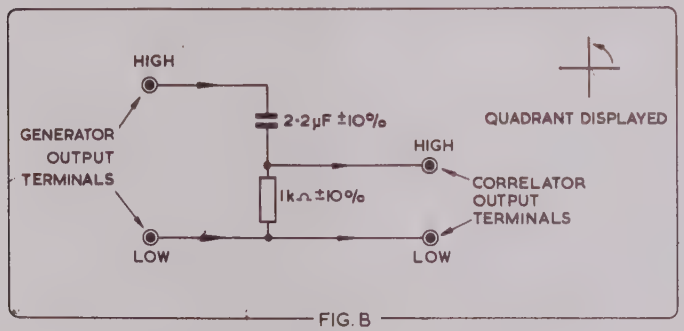


FIG. B

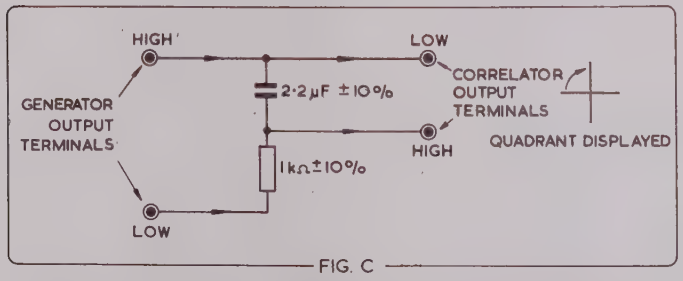


FIG. C

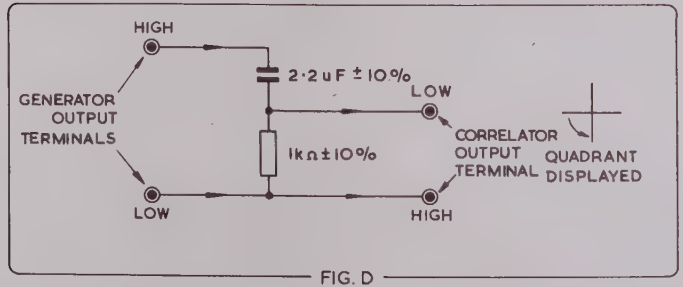


FIG. D

FIG. 5·2 PHASE SHIFT NETWORKS AND QUADRANTS DISPLAYED

(d) Plug-in p.c. extension board (S.E. Laboratories Board No. 30687). This board is provided to enable the serviceman to gain access to the test points referred to in the following procedure.

NOTE: For the following checks and adjustments, the top cover must be removed from the SM2001 (see Para. 2.1.).

4.3. Power Supply

(a) Connect the digital voltmeter to each power supply rail, in turn, and check for the appropriate reading as listed below. Adjust the appropriate potentiometer, if necessary. Adjustments can only be made on power units fitted to SM2001 instruments, serial nos. /001 to /006. Subsequent instruments (ser. no. /007 onwards) can only be checked to the values stated in brackets in the table below.

Generator Supply	Adjust (Ser. No. 001 to 006)	Indicated Reading
$+5V_g$ (+5V)	–	+5V, (+5V)
$+17V_g$ (+18V)	RV2 (board B30704)	+17V ± 0.1V, (+18V)
$-17V_g$ (−18V)	RV1 (board B30704)	−17V ± 0.1V, (−18V)
Earthy Supply		
$+5V_e$ ((+5V)	–	+5V, (+5V),
$+17V_e$ (+18V)	RV4 (board B31471)	+17V ± 0.1V, (+18V)
$-17V_e$ (−18V)	RV3 (board B31471)	−17V ± 0.1V, (−18V)
+250V	–	250V ± 10V
Correlator Supply		
$+5V_c$ (+5V)	–	+5V, (+5V)
$+17V_c$ (+18V)	RV6 (board B31471)	+17V ± 0.1V, (+18V)
$-17V_c$ (−18V)	RV5 (board B31471)	−17V ± 0.1V, (−18V)

4.4. Generator Controls and Display Indicators Check

(a) Switch-on the SM2001.

(b) Set the EXT PROG and EXT SYNC push-buttons to off (integral indicators extinguished).

(c) Depress the SET F push-button and operate the UP:DOWN push-buttons until the displays are cleared. Check that each decade counts up and down through zero set to 999.

(d) Depress the SET V push-button and operate the UP:DOWN push-buttons until the displays are cleared. Check that each decade counts up and down through zero set to 999.

(e) Depress the SET F push-button. Depress the FREQUENCY RANGE UP push-button until the display reads 999Hz.

(f) Depress the FREQUENCY RANGE DOWN push-button once, and check that the display reads 99.9Hz.

(g) Check that for successive operations of the DOWN push-button, the display reading changes as shown below.

DOWN push-button Operation	Display Reading
Second Time	9.99Hz
Third Time	999Hz x 10^{-3}
Fourth Time	99.9Hz x 10^{-3}
Fifth Time	9.99Hz x 10^{-3}

(h) Depress and hold the FREQUENCY RANGE UP push-button and check that the sequence, 9.99Hz x 10^{-3}, 99.9Hz x 10^{-3}, 999Hz x 10^{-3}, 9.99Hz, 99.9Hz, 999Hz, is followed automatically. Release the UP push-button.

(j) Depress the SET V button and select 100mV on the AMPLITUDE control. Check the display reads 99.9mV

(k) Select the 1V range and check the display reads ... ... 999 mV

Select the 10V range and check the display reads 9.99V

(m) Using the table below, check that the front panel indicators light up in the sequences shown (by the asterisks) for switch positions indicated.

Switch Positions					Centre Display						R.H. Display						Quad. Display
Measure-ment Sw. Range	Amp-litude Sw. Posn.	C	P	P/dB	Pol ±	V	mV	x10^{-3}	GN	dB	Pol ±	j	V	mV	x10^{-3}	O	
0.1V	All	*			*		*				*	*		*			
1V 10V 100V	All	*				*					*	*	*				
Ratio																	
4, 3	All	*			*				*		*	*					
2, 1	10V	*						*	*		*	*			*		
1	1V	*			*			*	*		*	*			*		
2	1V	*			*				*		*	*					
2,1	100mV	*			*				*		*	*					
0.1V	All		*				*									*	*
1V 10V 100V	All		*			*										*	*
4, 3	10V		*						*							*	*
2, 1	10V		*					*	*							*	*
1	1V		*					*	*							*	*
1	100mV		*						*							*	*
0.1,1V, 10V 100V	All			*	*					*						*	*
4, 3, 2, 1	10V 1V 100mV			*	*				*	*						*	*

4.5. Crystal Oscillator Calibration Check (Board G)

(a) Connect the timer/counter between test point TP1 on the crystal oscillator and DRM board (G) and OV_e (chassis).

(b) Check that the clock frequency is 6.74MHz ± 10Hz.

(c) Using the oscilloscope monitor test point TP4 on the digital oscillator board (C). Check that, when the generator frequency is set to 999Hz, a squarewave of 50:50 mark space ratio is displayed, having a period of 1 ms.

4.6. Voltage Control (Generator) Board A (SKT A) — Digital-to-Analogue Converter Adjustment

S.E.L. Board No: E31478
S.E.L. Assy. No: B31480

NOTE The following steps (a) to (h) must also to be used to check the digital-to-analogue converter section on voltage control (correlator) board U, but only when that point in the setting-up procedure has been reached.

(a) Connect the digital voltmeter across the output (pin 6) of IC8 and test point TP3 (OV_g)

(b) Set the generator voltage to read 0.00V on the L.H. display.

(c) Adjust potentiometer RV1 on board A for a digital voltmeter reading of OV,

(d) Increase the generator voltage to 0.01V and note the digital voltmeter reading. This is equivalent to 1 bit.

(e) Increase the generator voltage to 0.02V and check that the digital voltmeter reads twice the reading obtained in step (d) ± 1 mV.

(f) Increase the generator voltage to 0.04V and check that the digital voltmeter reads twice the reading obtained in step (e) ± 1 mV.

(g) Increase the generator voltage to 0.08V and check that the digital voltmeter reads twice the reading obtained in step (f) ± 1 mV.

(h) Continue to increase the generator voltage in BINARY sequence to 512, and check that, the digital voltmeter reading doubles for each binary step ± 1 bit.

4.7. Digital-to-Analogue Converter (Generator) Board B (SKT B) — Adjustments

S.E.L. Board No: E30686
S.E.L. Assy. No: B30706

(a) Connect the digital voltmeter across the output of IC1, (test point TP3) and OV_g (test point TP2).

(b) Set the generator voltage to read 000V on the L.H. display. Depress the STOP 0^o push-button.

(c) Adjust potentiometer RV3 on board B for a digital voltmeter reading of 0 ± 1 mV.

(d) Depress the STOP 180^o push-button. Adjust potentiometer RV2 on board B for a reading 0V ± 1 mV. If this cannot be obtained, change the value of R79 (68k to 100k)

(e) Depress the STOP 90^o push-button. Adjust potentiometer RV5 for a reading of 0V ± 1 mV.

(f) Depress the STOP 270° push-button. Check that the digital voltmeter indicates OV ± 1mV.

(g) Check, again, the STOP 0°, 90°, 180° and 270° and re-adjust readings to 0V ± 1mV.

(h) Set the generator voltage to indicate 9.99V in the L.H. display. Depress the STOP 90° push-button. Note that the reading indicated by the digital voltmeter is of positive polarity (the exact value is not important at this stage).

(k) Depress the STOP 270° push-button. Check that the reading on the digital voltmeter is of negative polarity and the same value as in step (h) above.

(m) Adjust potentiometers RV4 (for 90° and 270° polarities) and RV1 (for 270° only) until the readings of both polarities are the same ± 10mV.

4.8. **Voltage Control (Generator) Board A (SKT A) – Output Amplifier Adjustment**

S.E.L. Board No: E31478
S.E.L. Assy. No: B31480

(a) Connect the digital voltmeter across R53 on board A.

(b) Depress the STOP 0° push-button. Adjust potentiometer RV3 (on board A) until a reading of 150 mV ± 20mV is obtained.

(c) Disconnect the digital voltmeter and connect it across the GENERATOR OUTPUT terminals. Set the AMPLITUDE selector to the 100mV range.

(d) Adjust potentiometer RV2 (on board A) until the digital voltmeter indicates OV. If this reading cannot be obtained, change the value of resistor R41 (12.1k ± 1%).

(e) Set the AMPLITUDE selector to the 1V range. Check for a reading of OV ± 1 mV.

(f) Set the AMPLITUDE selector to the 10V range. Check that the reading is OV ± 1mV.

(g) With the 10V amplitude range selected, set the generator voltage to 9.99V (as indicated on the generator display). Depress the STOP 90° push-button.

(h) Adjust potentiometer RV6 on digital-to-analogue converter board (B) for a digital voltmeter reading of + 9.99V ± 5mV. If these limits cannot be obtained, refer step (k) below.

(j) Depress the STOP 270° push-button. Check that the digital voltmeter indicates –9.99V ± 5mV. If the reading is outside these limits, refer to step (k) below.

(k) To obtain limits of ±5mV in steps (h) and (j) above, re-adjust potentiometers RV4 and RV1 on board B as given in step 4.7 (m), with the digital voltmeter connected to the GENERATOR OUTPUT terminals.

4.9. **Digital Oscillator (Correlator) Board S (SKT S) – Checks**

S.E.L. Board No: E30697
S.E.L. Assy. No: B30930

(a) Connect the oscilloscope across test point 4 (bistable 22/8, $\overline{Q}$ output) and OV (test point 7) on board S.

(b) Depress the RUN push-button and set the generator frequency to 99.9Hz.

(c) Check that a squarewave of frequency 99.9Hz is displayed on the oscilloscope.

(d) With the oscilloscope triggered from TP4, set the HARMONIC selector to position 2. Check that the frequency of the displayed squarewave is 200Hz.

(e) Set the HARMONIC selector to each position in turn and check that the displayed squarewave frequency for each position is as listed below.

HARMONIC Selector posn.	Frequency (Hz)
3	300
4	400
5	500
6	600
7	700
8	800
9	900

(f) Set the HARMONIC Selector to position1 and increase the generator frequency to 999Hz.

(g) Monitor test point TP5 (on board S), using the oscilloscope. Check that a train of pulses is displayed, the p.r.f. of which is varying according to the sine of the generator waveform.

(h) Monitor test point TP6 (on board S), for a train of pulses, the p.r.f. of which is varying according to the cosine of the generator waveform..

4.10. Voltage Control (Correlator) Board U (SKT U)

S.E.L. Board No: E30685
S.E.L. Assy. No: B30932

4.10.1. *Digital-to-Analogue Converter Section.* To check and adjust this section, carry out the procedure given in Para 4.6 (a) to (h) inclusive.

4.10.2. *Output Switching Check*

(a) Connect the digital voltmeter between board pin 47 and OV_c (TP3) on board U.

(b) Set the MEASUREMENT Selector to an ABSOLUTE (any range) position. Check that the digital voltmeter indicates +9V (approx.).

(c) Set the MEASUREMENT selector to a RATIO (any range) position. Check that the indicated reading is the same as the generator output voltage amplitude.

4.11. Analogue-to-Digital Converter (Correlator) Board V (SKT V)

S.E.L. Board No: E 32414
S.E.L. Assy No: B30933

(a) Set the generator output voltage to 9.99V, as displayed on the L.H. display. Set the MEASUREMENT selector to the ABSOLUTE 10V range. Depress the STOP 0^{O} push-button.

(b) Connect the GENERATOR OUTPUT terminals directly to the CORRELATOR INPUT terminals (HIGH to HIGH, LOW to LOW).

(c) With the oscilloscope (set to DC input coupling), monitor pin 7 of IC16. Adjust potentiometer RV1 (on board V) until the output of IC16 is symmetrical about zero.

4.12. Digital-to-Analogue Converter (Correlator) Board T (SKT T)

S.E.L. Board No: E32434
S.E.L. Assy No: B30931

(a) Set the MEASUREMENT Selector to RATIO 3. Set the generator output voltage to 000V.

(b) Connect the digital voltmeter across test point TP1 and test point TP3 (OV_c). Adjust potentiometer RV1 until the digital voltmeter indicates OV.

(c) Connect the digital voltmeter across test point TP2 and test point TP3 (OV_c). Adjust potentiometer RV3, for a digital voltmeter reading of OV.

(d) Connect the GENERATOR OUTPUT terminals to the CORRELATOR INPUT terminals (HIGH to HIGH, LOW to LOW). Set the generator output voltage to 9.99V and the output frequency to 999Hz.

(e) Depress the MEASURE push-button, repeatedly, while adjusting potentiometer RV2 (on board T), until the centre display reads 1.000.

(f) Set the MEASUREMENT selector to ABSOLUTE 10V.

(g) Depress the MEASURE push-button, repeatedly, while adjusting potentiometer RV2 (on board U) until the centre display reads 9.99V.

4.13. Linearity Check

(a) Set the generator output voltage to 9.99V and frequency to 999Hz. Connect the GENERATOR OUTPUT terminals to the CORRELATOR INPUT terminals (HIGH to HIGH, LOW to LOW).

(b) Decrease the generator output voltage in 1V steps (to 0.99V) and depress the MEASURE push-button at each step. Check that, each time the MEASURE push-button is depressed, the centre display reading is updated to agree with the new generator voltage setting.

(c) Decrease the generator output voltage (from 0.99V) in 0.1V steps to 0.59V. Check that the centre display is updated at each step, when the MEASURE push-button is depressed. Check that the readings on the (generator) L.H. display and centre display agree to within 0.1% (1 bit $\pm$ 0.5% of reading).

(d) Decrease the generator output voltage (from 0.59V) to 0.09V in 0.1V steps. Check that the reading on the centre display is updated to agree with the generator display each time the MEASURE push-button is depressed. Check that the readings between displays always agree to within $\pm$ 2 bits.

(e) Decrease the generator output voltage (from 0.09V) to 0.00V in 0.1V steps. Check that the centre display is updated to agree with the L.H. display each time the MEASURE push-button is depressed. Check that the readings between displays always agree to within $\pm$ 2 bits.

(f) If the limits, stated in steps (b) to (e) above, cannot be obtained change the value of the fitted S.O.T. capacitors C5, C6 or C7. Fit S.O.T. capacitors where none are fitted. The values of these must always be within the range 10pF to 47pF.

5. INTERNAL CHECKS AND ADJUSTMENTS – SM2002

The following procedure concerns the optional, external synchronisation boards, J and H.

Test Equipment Required

(a) Frequency Response Analyser SM2001. This must be the parent unit into which the reference synchroniser SM2002 is normally fitted. The SM2001 must be known to be serviceable as checked-out in sub-section 4.

(b) Oscilloscope (S.E. Laboratories SM113 or similar)

(c) Sinewave Signal Source, with outputs from 1.99 mHz to 400Hz at 2V p-p

Input Amplifier and Balance Control Board J (SKT J)

S.E.L. Board No. E31495
S.E.L. Assy No. B31497

(a) Connect a link from the junction of R14, R12 and C7 to OV_e on board J.

(b) Connect a known signal source to the EXT SYNC INPUT and the chassis terminal on the rear panel of the SM2001.

(c) With the test oscilloscope, monitor pin 7 of IC18 on board J. Reduce the input voltage gradually and at the same time adjust potentiometer RV1, keeping the displayed squarewave symmetrical. Continue reducing the input voltage until adjustment of RV1 can no longer maintain the square-wave symmetrical. RV1 should now be at the optimum position.

(d) Disconnect the link, fitted in (a) above.

1/t Generator Board H (SKTH)

S.E.L. Board No. E31494
S.E.L. Assy No. B31496

(a) Connect a signal source, set to 9.90Hz at 2V p-p, to the EXT SYNC INPUT terminal and the chassis terminal on the rear panel of the SM2001. Depress the EXT SYNC push-button and check that the push-button lights-up.

(b) The generator display should now indicate the frequency of the external signal source, to an accuracy of 2%.

(c) Set the frequency of the external signal to 20Hz (2V p-p) and connect this to the SM2001 CORRELATOR INPUT terminals. The connections to the EXT SYNC INPUT socket should remain. Select 1V ABSOLUTE range on the MEASUREMENT selector.

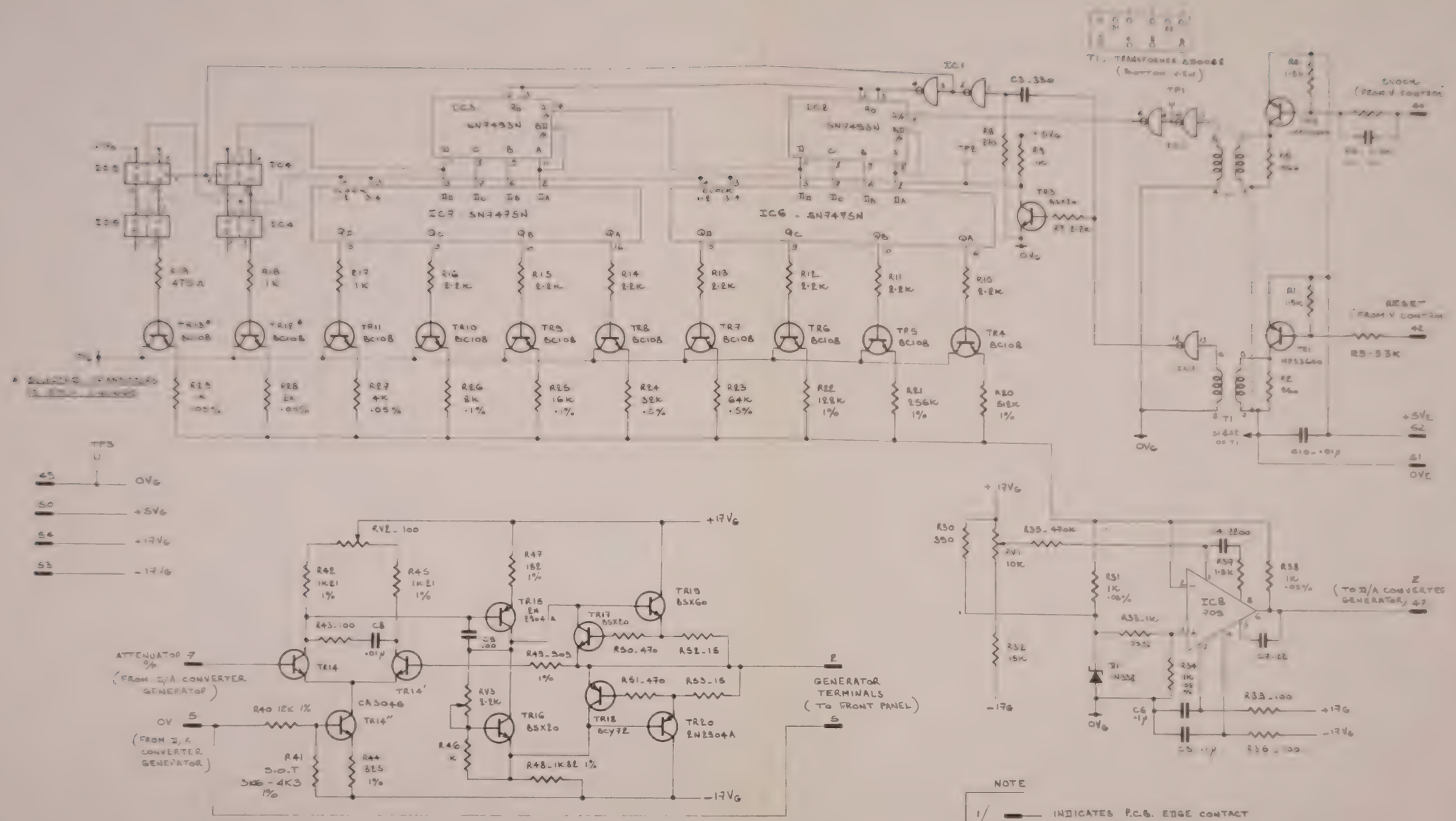
(d) Select POLAR display and depress the MEASURE push-button. Adjust potentiometer RV2 (on board J) until the centre display indicates a phase shift of less than $\pm 1^{o}$.

(e) Set the frequency of the external signal source to the values tabulated below and check that the phase shift is always less than $\pm 1^{o}$.

Signal Frequency	Phase Shift
400Hz	$< \pm 1^{o}$
1.99Hz	$< \pm 1^{o}$
199 mHz (milli-Hertz)	$< \pm 1^{o}$
19.9mHz	$< \pm 1^{o}$
1.99mHz	$< \pm 1^{o}$

SECTION 6

CIRCUITS AND COMPONENT LAYOUT DIAGRAMS



NOTE

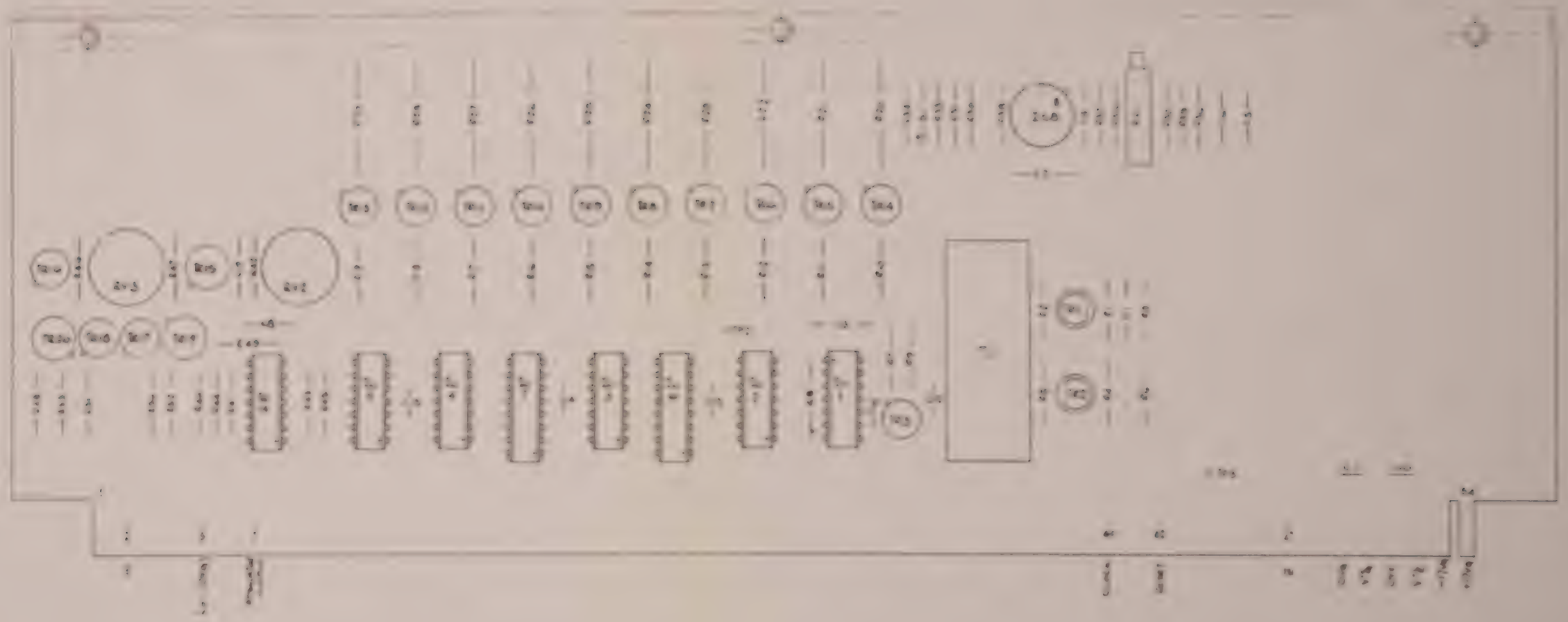
1/ ▬ INDICATES P.C.B. EDGE CONTACT

2/ C11 - C15 (NOT SHOWN) ARE .01μ DE-COUPLING CAPACITORS BETWEEN 0V6 & +5V6

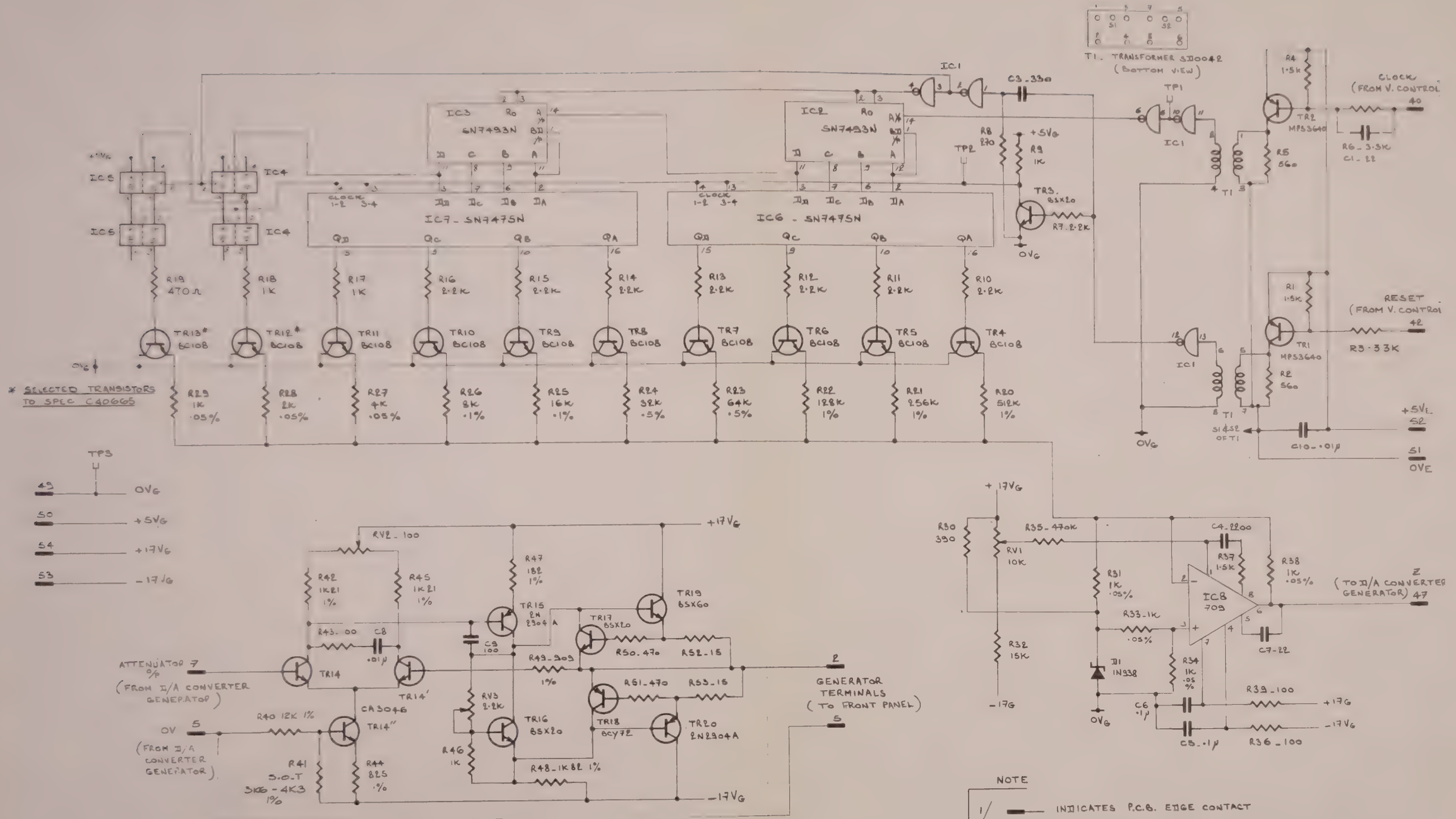
3/ POWER SUPPLY TO ICs:

	+5V6 PIN	- 0V6 PIN
SN7493N	4	11
SN7473N	5	12
SN7475N	5	12
ALL OTHER ICs. :	14	7

TITLE: VOLTAGE CONTROL GENERATOR — CIRCUIT DIAGRAM (BOARD 4)	JIG OR FIXTURE No	PARTS LIST No 3148D	DRAWING No B32669
	SCALE	SERIES No SM2001	



			B31480



NOTE

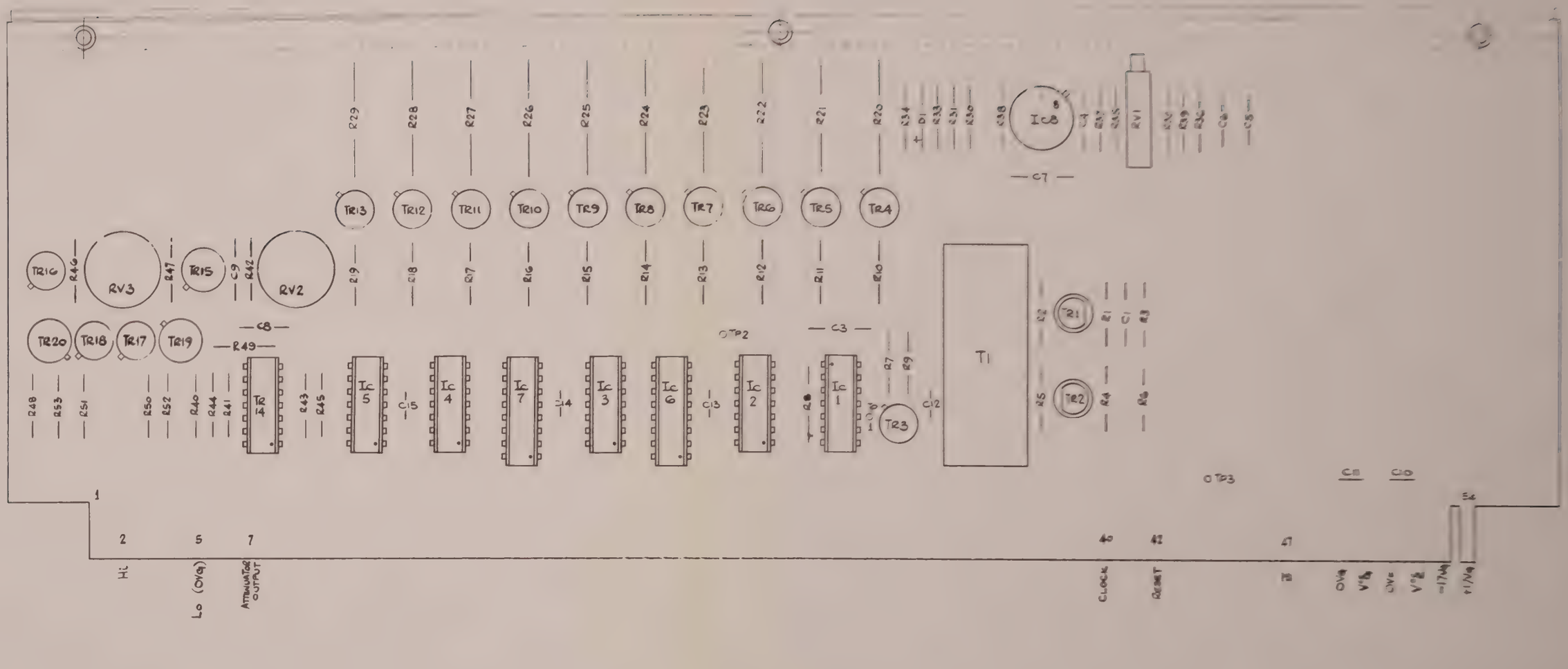
1/ ▬ INDICATES P.C.B. EDGE CONTACT

2/ C11 - C15 (NOT SHOWN) ARE .01μ DE-COUPLING CAPACITORS BETWEEN OVG & +5VG

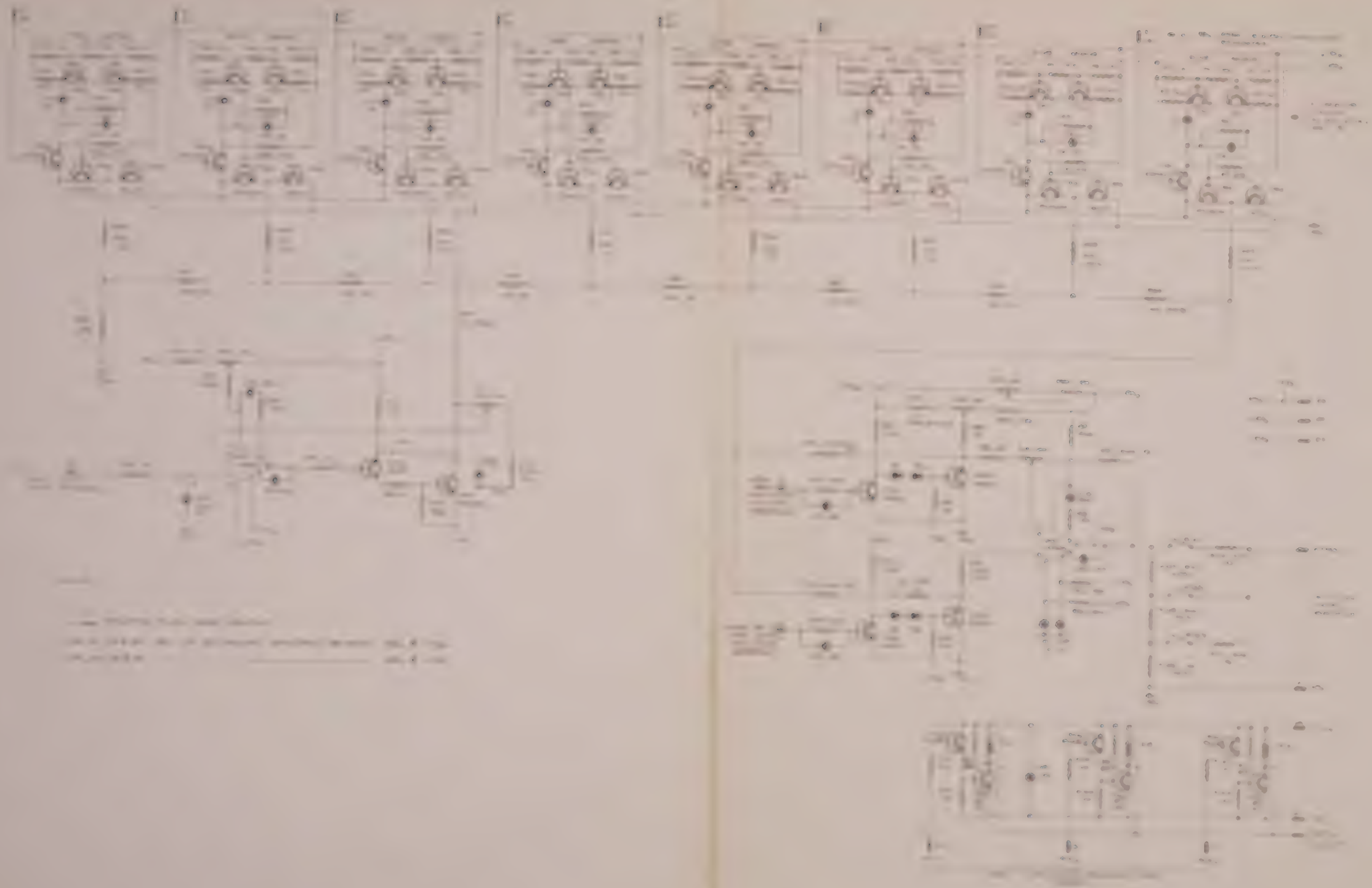
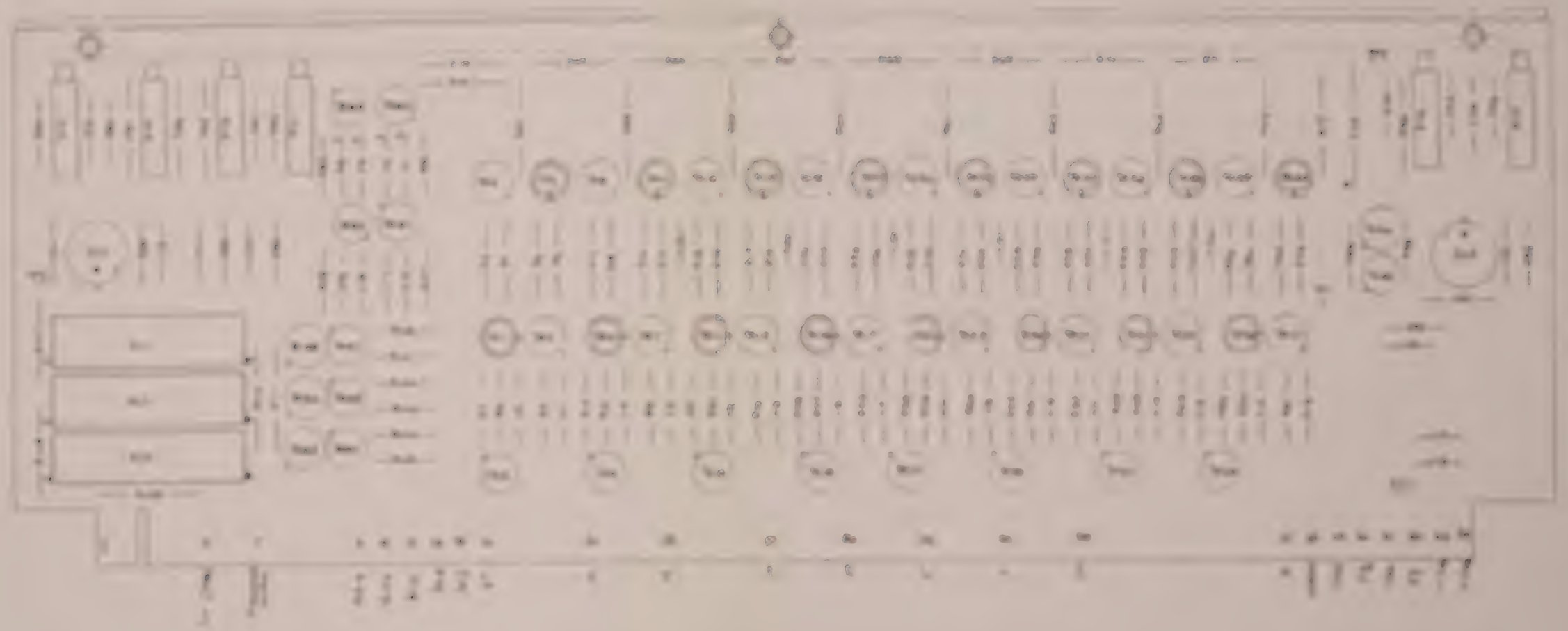
3/ POWER SUPPLY TO ICS:

	+5VG PIN 5	- OVG PIN 10
SN7493N	4	11
SN7473N	4	11
SN7475N	5	12
ALL OTHER ICS.	14	7

TITLE	JIG OR FIXTURE No	PARTS LIST No	DRAWING No
VOLTAGE CONTROL GENERATOR CIRCUIT DIAGRAM BOARD A		31480	B 32669
	SCALE	SERIES No SM2001	



TITLE VOLTAGE CONTROL (GENERATOR) P.C.B. ASSY. (BOARD A)	JIG OR FIXTURE No	PART'S LIST No 31480	DRAWING No B31480
	SCALE 2:1	SERIES No SM8001	



NOTE — INDICATES PCB EDGE CONTACT
C23 - C34 ARE ·01μF DE-COUPLING CAPACITORS BETWEEN +5V$_G$ & 0V$_G$
POWER SUPPLY TO ICs : SN74191N +5V$_G$ PIN16 , 0V$_G$ PIN 8
SN7473N —— PIN4 , —— PIN11
ALL OTHER ICs : —— PIN14 —— PIN7

SN74191N

SN7400N

SN74H30N

QUADRANTS (TO D/A. GENERATOR)

R14 - R25 = 1·5K
C6 - C11 = 22pF

SIN BECOSE O/Ps (TO D/A GENERATOR)

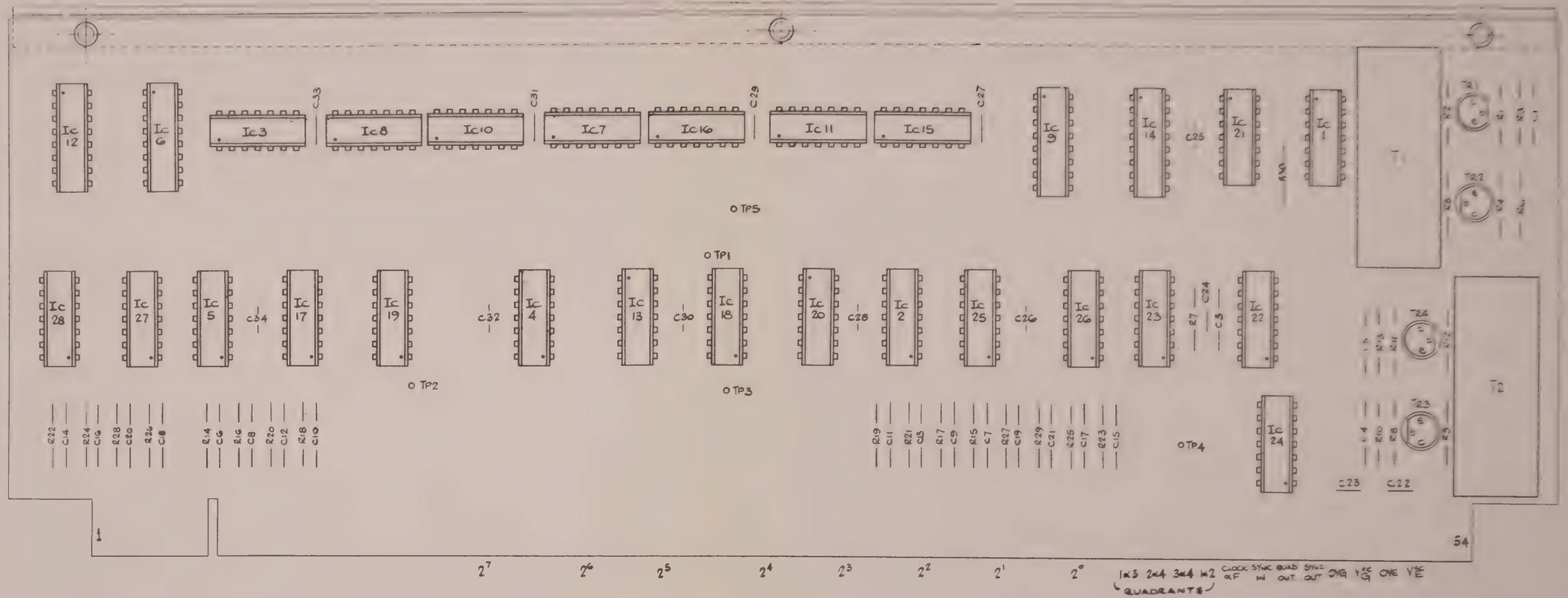
QUADRANTS O/p (TO CYCLES OF INTEGRATION CONTROL)

SYNC. OUT (TO BALANCE CONTROL & F. RANGE CONTROL)

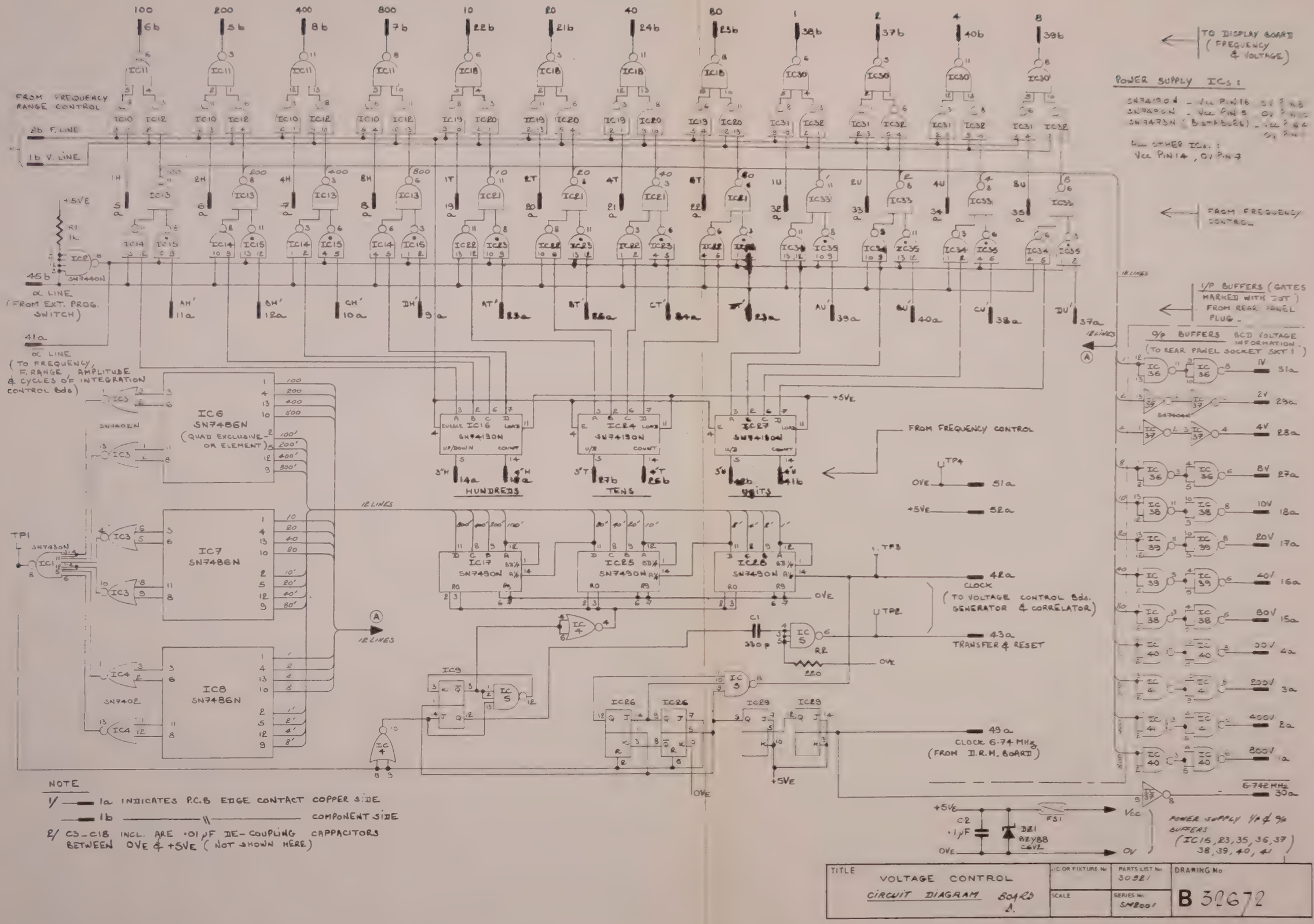
CLOCK xF 4G (FROM F RANGE CONTROL)

SYNC I/P 4G (FROM BALANCE CONTROL)

TITLE: DIGITAL OSCILLATOR GENERATOR CIRCUIT DIAGRAM BOARD C	JIG OR FIXTURE No	PARTS LIST No 30920	DRAWING No B 32671
	SCALE	SERIES No SM2001	



TITLE DIGITAL OSCILLATOR – SIN DECODE P.C.B. ASSY. (BOARD C)		PART LIST No. 30920	DRAWING No. B30920
	SCALE 2:1	SERIES No. SM 2001	

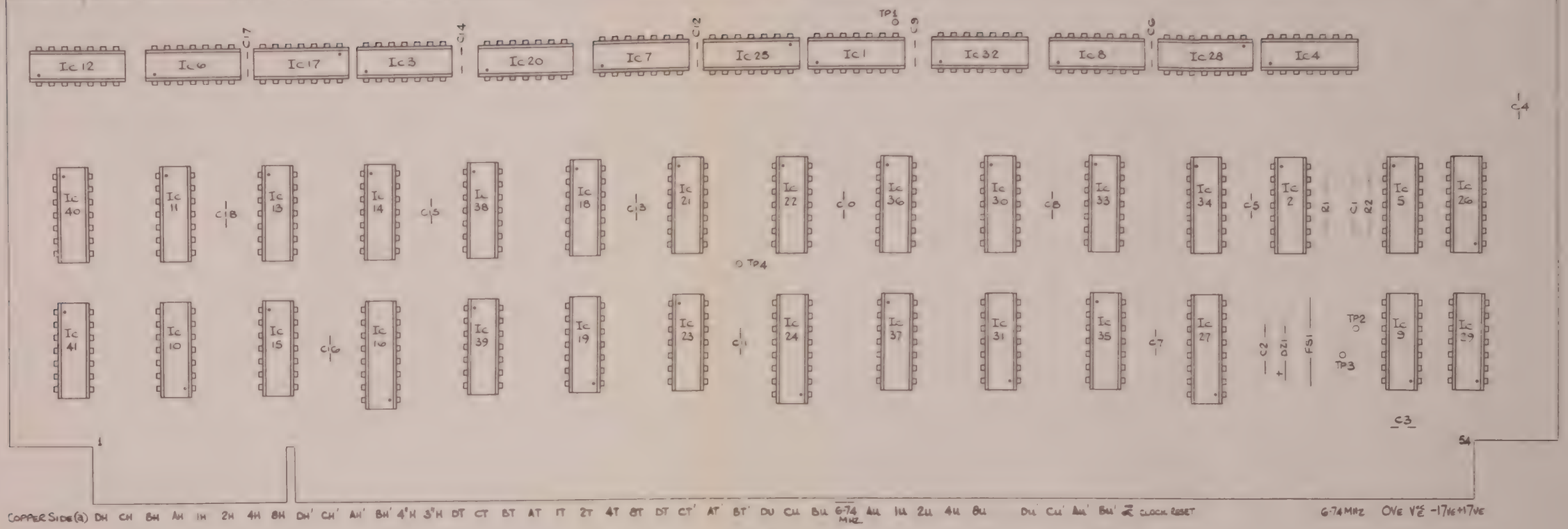


NOTE

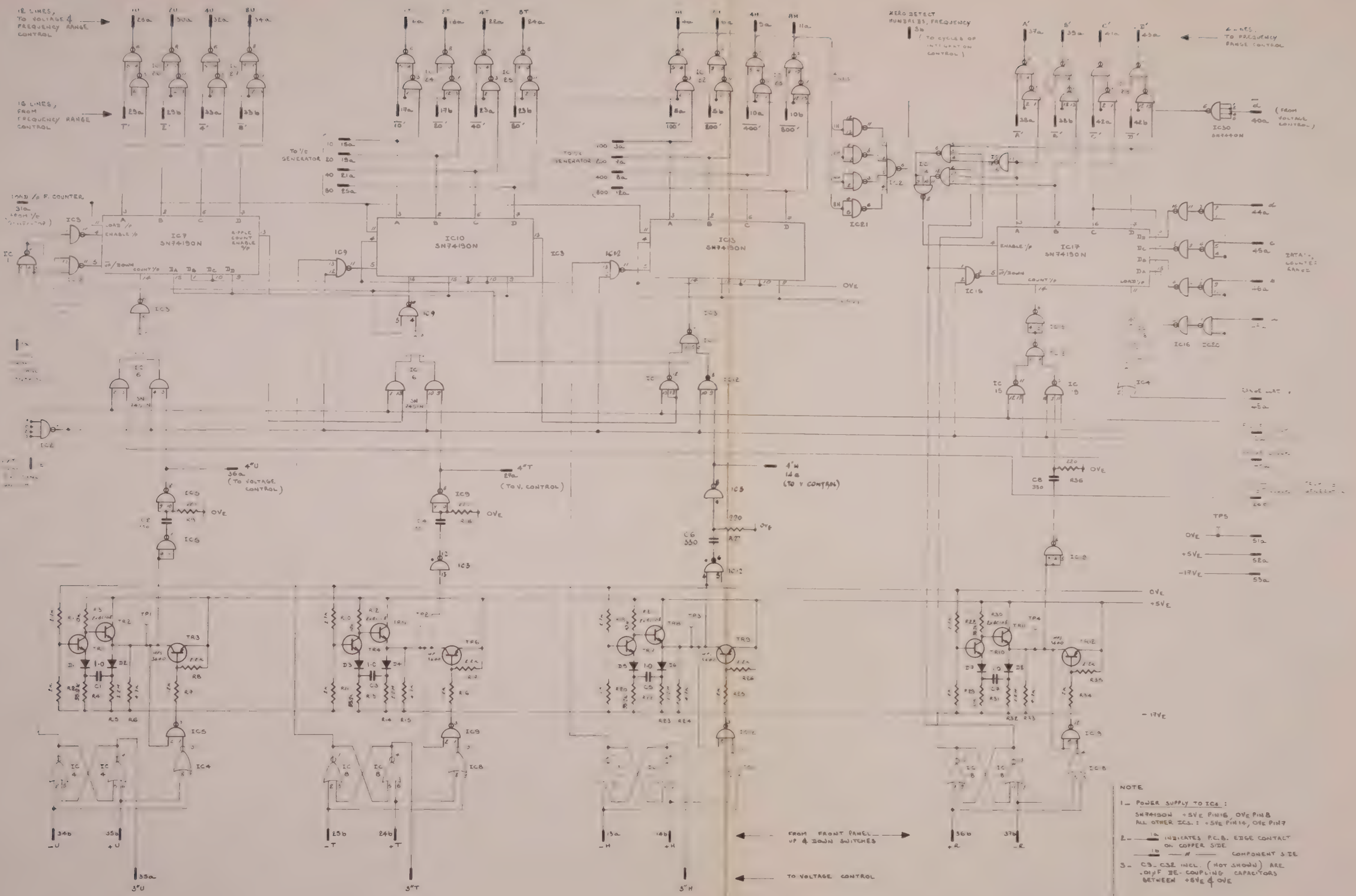
1/ —— 1a INDICATES P.C.B EDGE CONTACT COPPER SIDE
—— 1b —— " —— COMPONENT SIDE

2/ C3–C18 INCL. ARE ·01 μF DE-COUPLING CAPPACITORS BETWEEN OVE & +5VE (NOT SHOWN HERE)

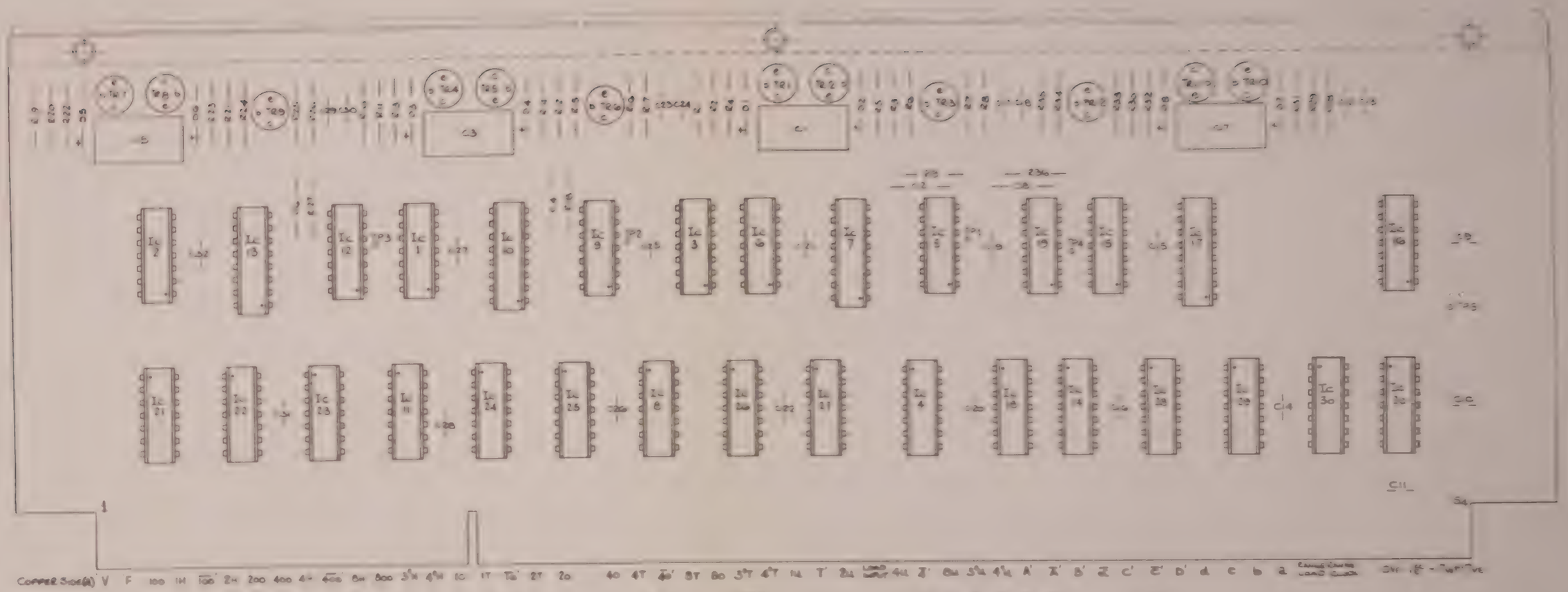
TITLE: VOLTAGE CONTROL CIRCUIT DIAGRAM Board A.	J/C OR FIXTURE No.	PARTS LIST No. 30921	DRAWING No. B 30672
	SCALE	SERIES No. SM2001	



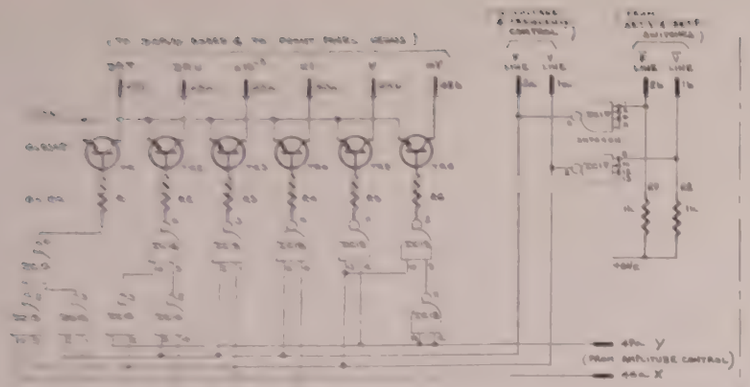
TITLE: VOLTAGE CONTROL P.C.B. ASSY. (BOARD D)	MOTOR FIXTURE No.	PARTS LIST No. 30921	DRAWING No. B30921
	SCALE 2:1	SERIES No. SM2001	

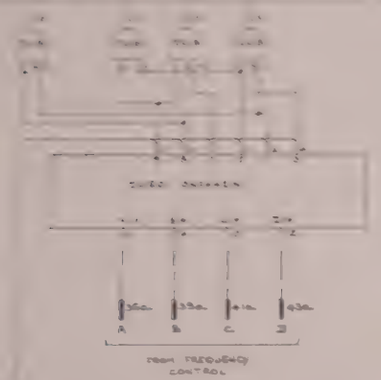


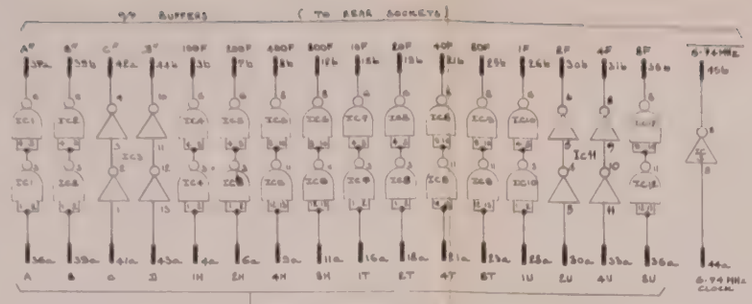
TITLE	JIG OR FIXTURE No	PARTS LIST No	DRAWING No
FREQUENCY CONTROL CIRCUIT DIAGRAM BOARD E		3032E	E32673
	SCALE	SERIES No SM2001	

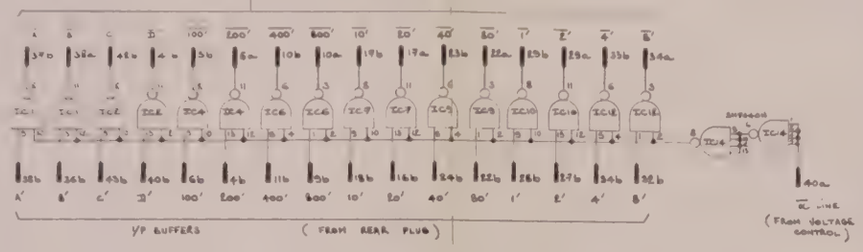


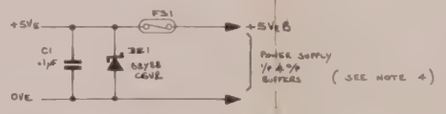
Plano key Access - Frequency & Tenths Address P.C.B. Assy. (Board 8)		30922	DRAWING No. B30922
	2:1	SM 2001	











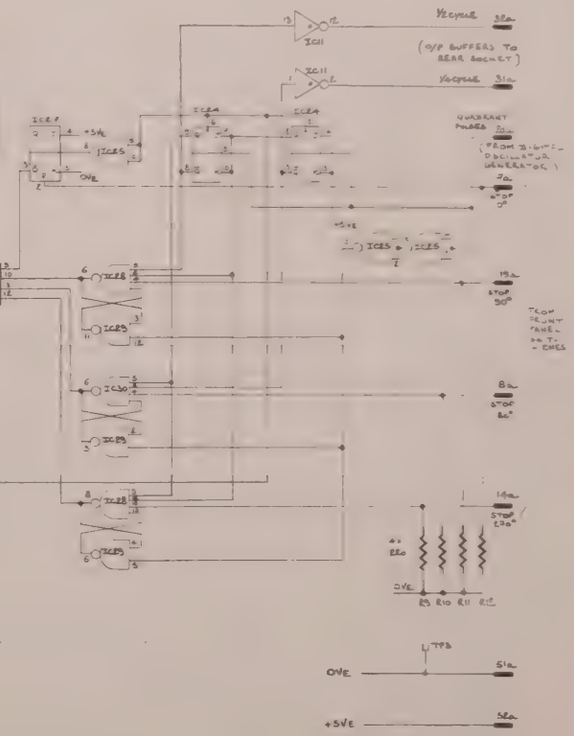
NOTE

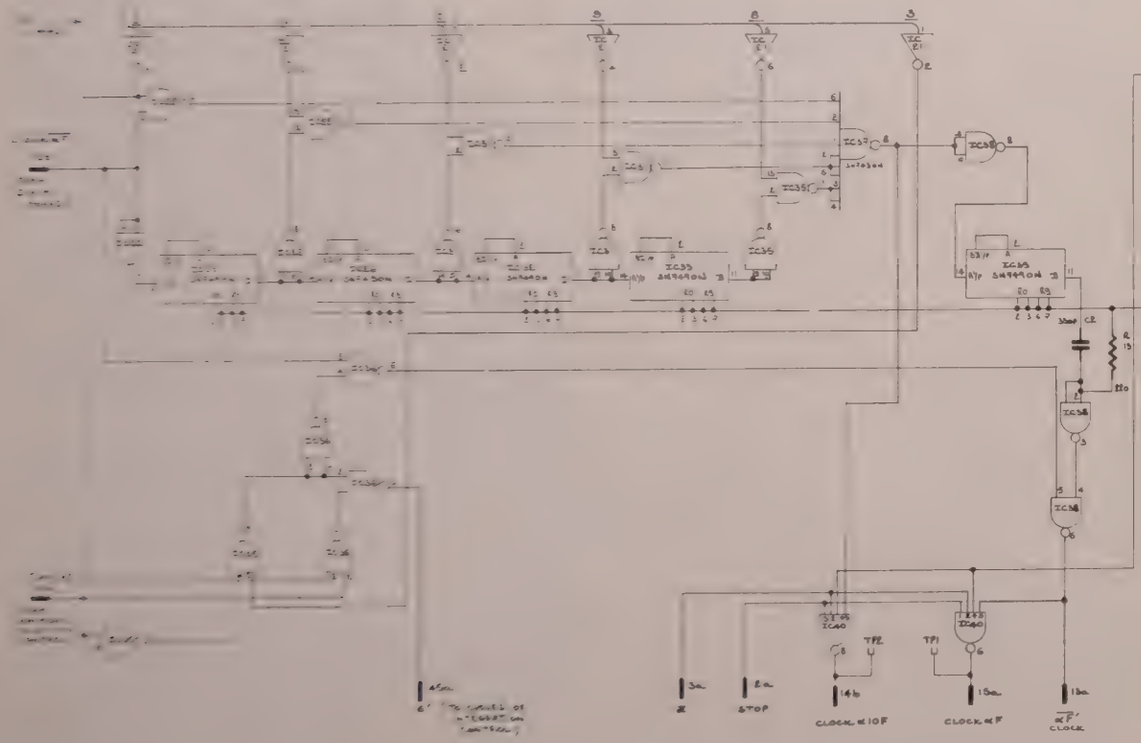
1/ —— 1a INDICATES P.C.B. EDGE CONTACT COPPER SIDE
—— 1b " " COMPONENT SIDE

2/ C6 – C16 (4Nos. ARE +0.1μF DE-COUPLING CAPACITORS) BETWEEN +5VE & 0VE (NOT SHOWN HERE)

3/ POWER SUPPLY IC Nos. 1 SN7430N +5VE – PIN 8, 0V. PIN 10
SN7473N (BISTABLES) +5V – PIN 4
0V – PIN 11
SN7440N +5VE – PIN 16, 0V. PIN 8
ALL OTHER ICs. : +5VE – PIN 14, 0V – PIN 7

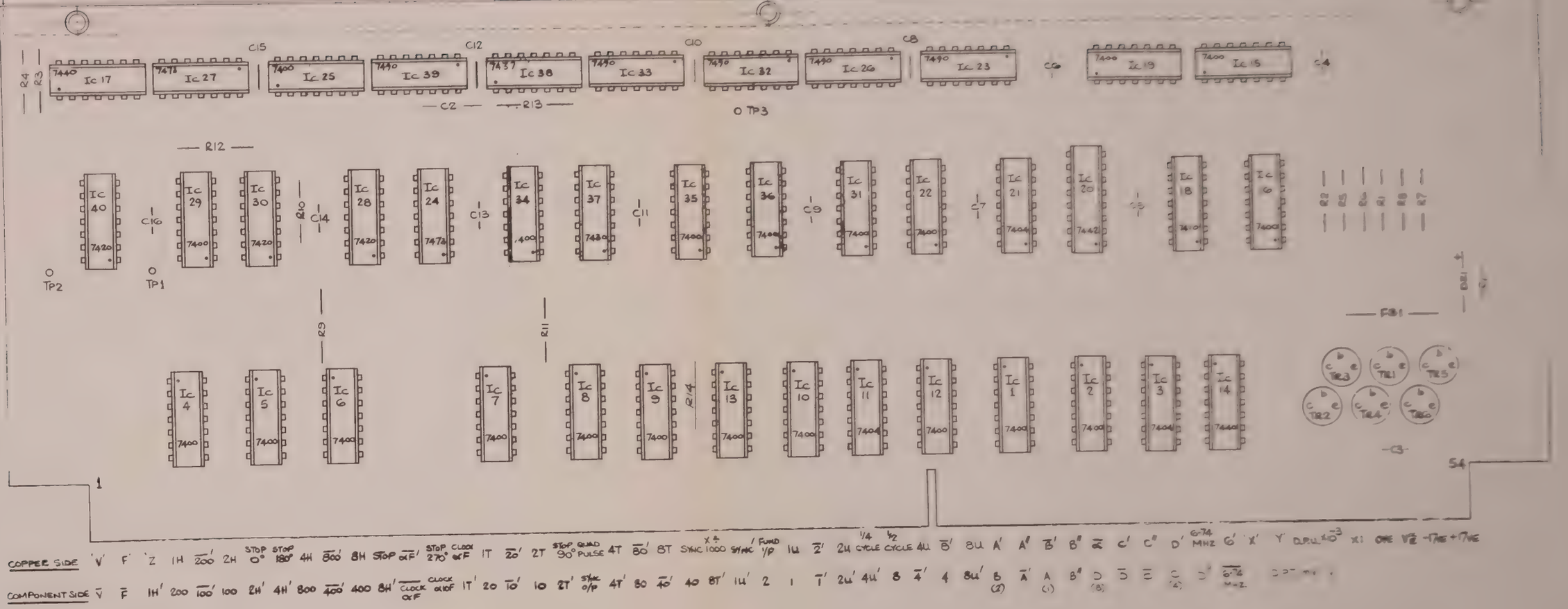
4/ GATES MARKED WITH BOT (IC11 & IC13) ARE BUFFERS AND ARE CONNECTED TO THE +5VE & 0VE AS IC1, IC2, IC3, IC4, IC5, IC6, IC7, IC8, IC9 IC10, & IC12



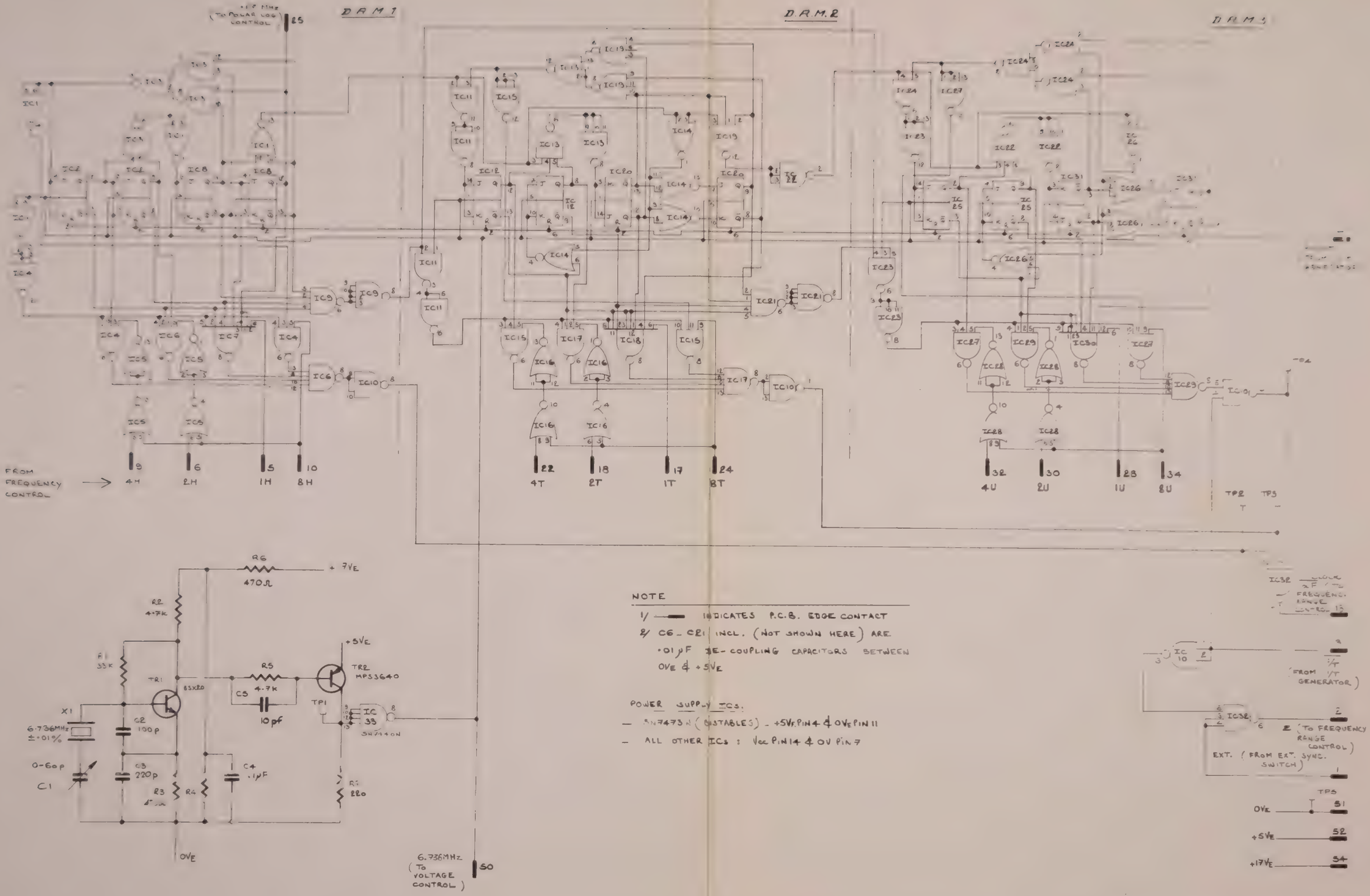


NOTE : CLOCK «F' & STOP – TO BALANCE CONTROL
CLOCK «F – TO DIGITAL OSCILLATOR GENERATOR
CLOCK «10F – TO HARMONIC SELECTION CONTROL
Z – FROM I.B.M. BOARD

TITLE: FREQUENCY RANGE CONTROL — CIRCUIT DIAGRAM BOARD F	JIG OR FIXTURE No	PARTS LIST No. 30923	DRAWING No. E32674
	SCALE	SERIES No. SMR001	


C15
C12
C10
C8
C6
C4
R4
R3
R12
R13
C2
TP3
TP2
TP1
C16
C14
C13
C11
C9
C7
C5
C1
R10
R9
R11
R14
R8
R7
R6
R5
R1
R2
C3
1
54
Ic 17
Ic 27
Ic 25
Ic 39
Ic 38
Ic 33
Ic 32
Ic 26
Ic 23
Ic 19
Ic 15
Ic 40
Ic 29
Ic 30
Ic 28
Ic 24
Ic 34
Ic 37
Ic 35
Ic 36
Ic 31
Ic 22
Ic 21
Ic 20
Ic 18
Ic 16
Ic 4
Ic 5
Ic 6
Ic 7
Ic 8
Ic 9
Ic 13
Ic 10
Ic 11
Ic 12
Ic 1
Ic 2
Ic 3
Ic 14
TR3
TR1
TR5
TR2
TR4
TR6
7400
7420
7430
7440
7442
7410
COPPER SIDE
COMPONENT SIDE

| | | |



NOTE

1/ —▬— INDICATES P.C.B. EDGE CONTACT

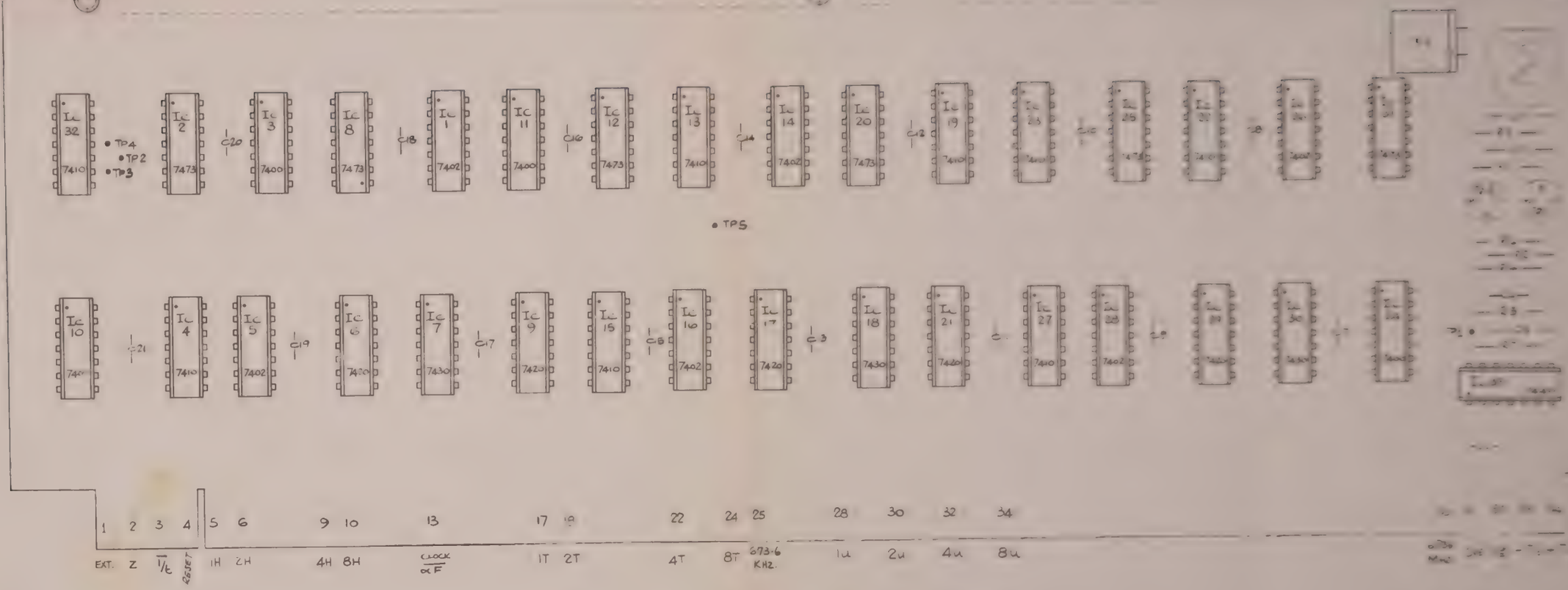
2/ C6 – C21 INCL. (NOT SHOWN HERE) ARE ·01μF DE-COUPLING CAPACITORS BETWEEN 0VE & +5VE

POWER SUPPLY ICs.

– SN7473 N (BISTABLES) – +5VE PIN 4 & 0VE PIN 11

– ALL OTHER ICs : Vcc PIN 14 & 0V PIN 7

TITLE: DECIMAL RATE MULTIPLIERS 6·736 MHz CLOCK CIRCUIT DIAGRAM Boyes G.	JIG OR FIXTURE No	PARTS LIST No 30984	DRAWING No B 32684
	SCALE	SERIES No SM2001	



TITLE DECIMAL RATE MULTIPLIER & 6·736 MHz CLOCK OSCILLATOR P.C.B ASSY BOARD 4		30924	B30924
	2	JM2001	

RESET B
TO S/N 1000 POLAR LOG & DISPLAY PCB)

INTEGRATION TIME
30
(TO POLAR CONTROL)

RESET A
(TO COS REGISTER & HARMONIC SELECTION CONTROL)

COMPONENTS
(FROM DIGITAL OSCILLATOR GENERATOR)

IC4 SN7490N
IC3 SN7490N
IC15 SN7490N
R9 R0

IC5 SN74190N
IC10 SN74190N
IC16 SN74190N
IC17
LOAD, COUNT, UP/DOWN, ENABLE, RIPPLE CT. I/P

IC29 SN74190N
IC30 SN74190N
IC33 SN74190N
IC34

OVE
+5VE
-17VE
TP10
51
52
55

TP2 TP3 TP4
42 39 35 32
E1 COS
RCE 1 COS
E2 COS
E3 COS
MMI COS
34
MMI SIN

FROM COS REGISTER

S LINES

TP6 TP7 TP8 TP9
41 37 36 31
E1 SIN
RCE 1 SIN
E2 SIN
E3 SIN
38
MMI SIN

FROM SIN REGISTER

(2 LINES FROM CYCLES OF INTEGRATION)

(6 LINES TO REAR PANEL SOCKET)
X0 X1 X2 X3

6 LINES (FROM F. CONTROL)

ZERO DETECT MONITORS (FROM F. CONTROL)
24

IC25 H
IC26 G
IC27 F
IC2 I

C4 1000
OVE

+5VE
FS
BZX 55/8.2 ZENER
C5 .1μ
OEV

IC44 SN7404
+5VE

R7 2.2K
TR5 MPSA 5640
AUTO
R15 220
C27
.01
R8 2.2K
OVE

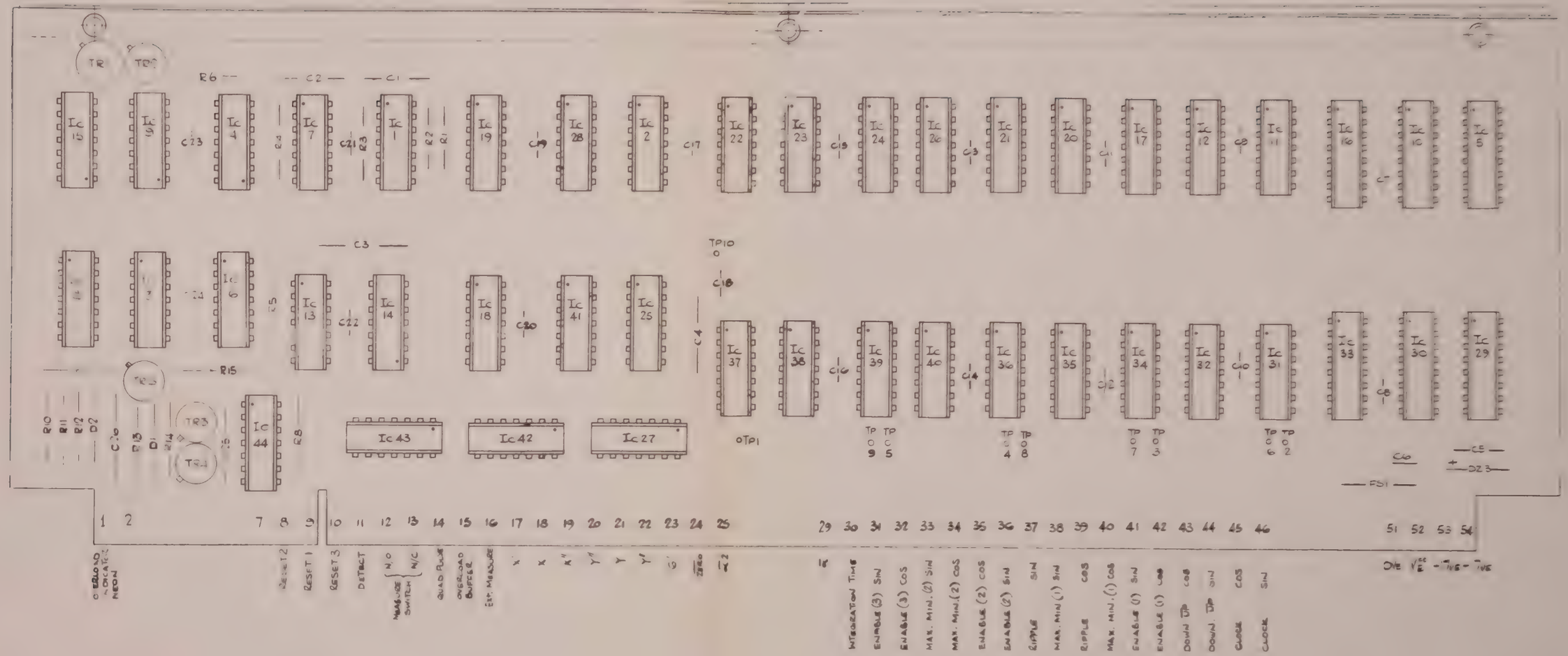
TR4 BC108
TR5 BC108
R9 3.01K
R10 2.74K
R11 2.1K
R12 10K
R13 1.2M
R14 4.7K
C25 1000P
D1 IN914
D2 IN914
C26 6.8μ
BLANKING

R1 8.7K
TR2 BC178
TR1 2N5963
OVE
OVERLOAD INDICATOR

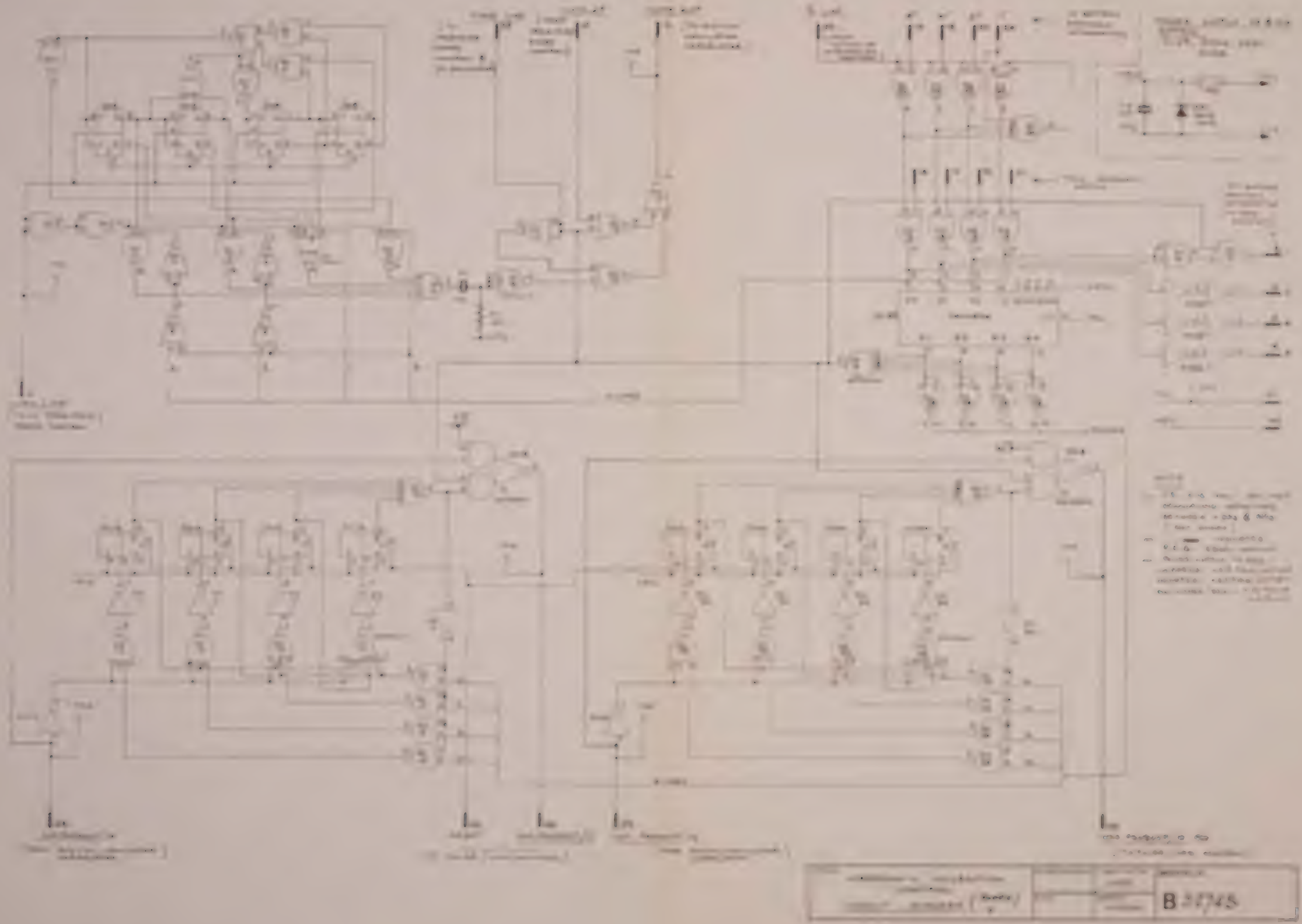
NOTE

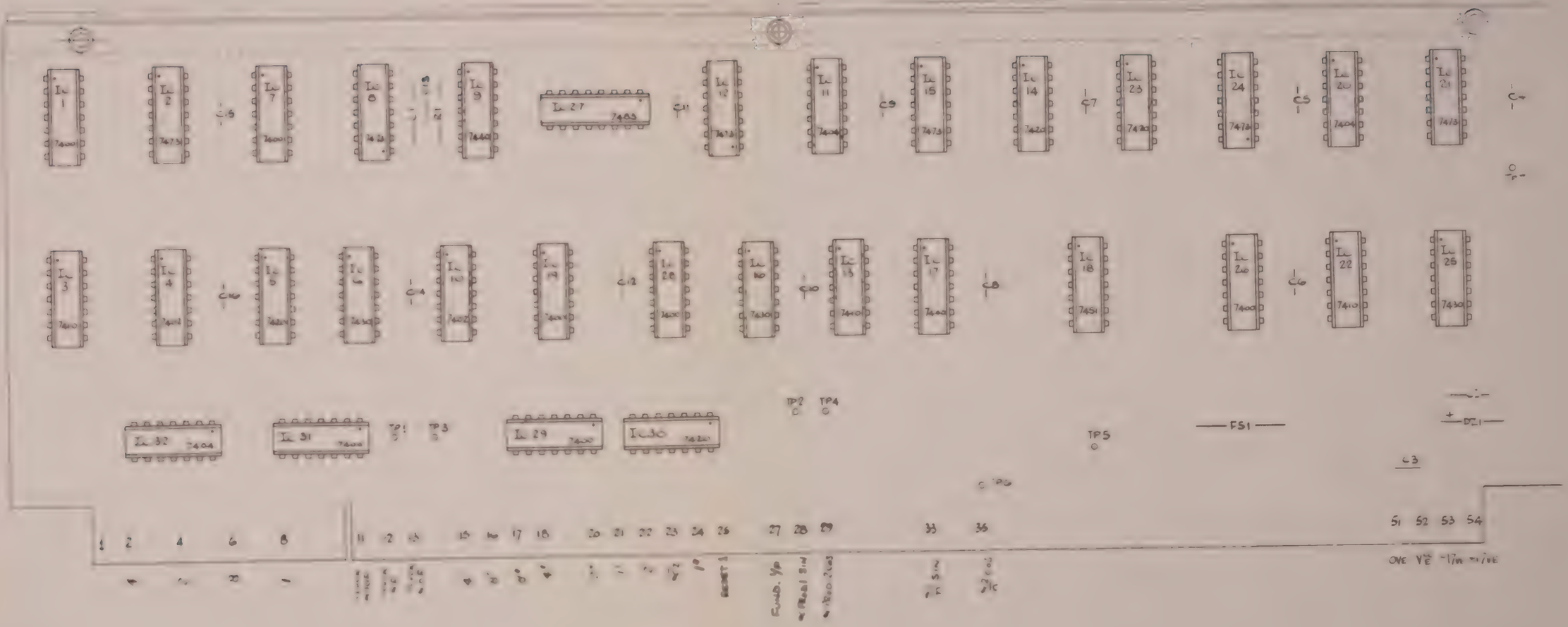
1. INDICATES PCB EDGE CONTACT
2. C6 - C24 INCL. (NOT SHOWN) ARE .01μF DE-COUPLING CAPACITORS BETWEEN OVE & 5VE
3. POWER SUPPLY TO I C s
   - SN 74190N : +5VE PIN 16 - OVE PIN 8
   - SN 7490N : — PIN 5 — PIN 10
   - SN 7478N — PIN 4 — PIN 11
   - ALL OTHER I Cs — PIN 14 — PIN 7

TITLE: CYCLES OF INTEGRATION CONTROL CIRCUIT DIAGRAM (BOARD K)	JIG OR FIXTURE No.	PARTS LIST No. 30925	DRAWING No. E 32746
	SCALE	SERIES No. SM2001	



TITLE CYCLES OF INTEGRATION DIVIDER CONTROL P.C.B. ASSY. BOARD K	JIG OR PICTURE No	PARTS LIST No 30825	DRAWING No B30925
	SCALE 2:1	SERIES No SM2001	





HARMONIC SELECTION CONTROL P.C.B. ASSY. BOARD 6		B30926	DRAWING No. B30926
	2:1	SM2001	

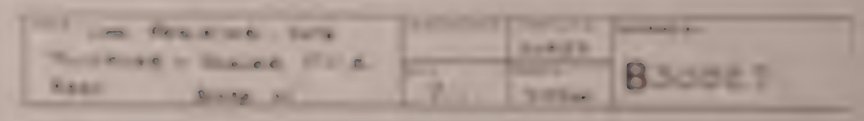
NOTE.

1/ ▬ INDICATES P.C.B. EDGE CONTACT

2/ C13 - C29 INCL. ARE .01μF DE-COUPLING CAPACITORS BETWEEN 0VE & +6VE (NOT SHOWN ON THIS CIRCUIT)

3/ POWER SUPPLY TO ICs. :
— SN74130N : +6VE - PIN16, 0VE PIN8
— SN7473N (BISTABLES) : +6VE PIN 4, 0VE PIN 11
— ALL OTHER ICs. : +5VE PIN 14, 0VE PIN7

TITLE	JIG OR FIXTURE No	PARTS LIST No	DRAWING No
COS REGISTER CIRCUIT DIAGRAM BOARD M.	SCALE	30927 SERIES No SM2001	B32675


8 sheet

NOTE

1/ — INDICATES P.C.B. EDGE CONTACT

2/ C13 - C81 INCL. (NOT SHOWN) ARE .01 μF DE-COUPLING CAPACITORS BETWEEN +5V£ & 0V£

3/ POWER SUPPLY TO IC's :

SN74150N & SN74181N	+5V£ PIN 16 ;	0V£	PIN 8
SN7473N	+5V£ PIN 4 ;	0V£	PIN 11
SN7496N	+5V£ PIN 5 ;	0V£	PIN 13
ALL OTHER IC's	+5V£ PIN 14 ;	0V£	PIN 7

(6 LINES TO CYCLES OF INTEGRATION CONTROL)

SET IN 2

ES (FROM POLAR LOG CONTROL)

0V£

IC15 SN74150N

IC 14 SN74181N

LINES 1S, 2S, 4S ... 800S, 1000S GO TO THE DISPLAY BOARDS

IC26 SN7430N

+5V£

IC25 SN7420N

4 LINES

IC16

IC31

IC30

IC29

IC28

IC27

IC 40

IC 39

IC 38

IC 37

IC 36

IC 35

IC 34

IC 33

IC 32

TP3 TP2 TP1

TP4

+5V£

4 LINES FROM POLAR LOG CONTROL

S SERIAL COUNTER

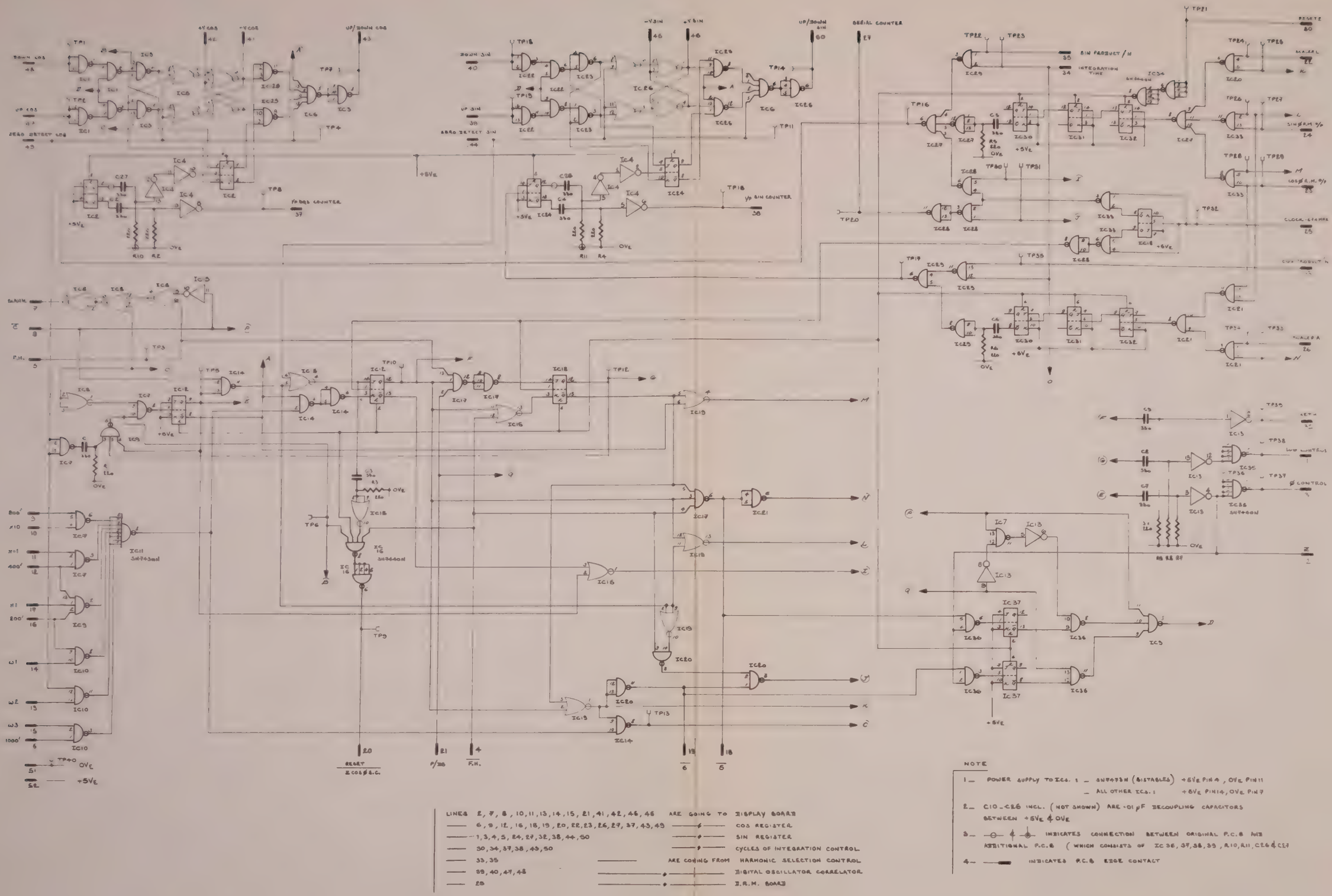
4S RESET ... CYCLES OF INTEGRATION

2S SINE R.M.S.

LINK TO APPROPRIATE CONTROL LINE

Ø CONTROL LOG CONTROL

TITLE: SIN REGISTER CIRCUIT DIAGRAM BOARD N		30928	DRAWING B52676
		SM2001	



LINES 2, 7, 8, 10, 11, 13, 14, 15, 21, 41, 42, 46, 46 ARE GOING TO DISPLAY BOARD
6, 9, 12, 16, 18, 19, 20, 22, 23, 26, 27, 37, 43, 49 — COS REGISTER
1, 3, 4, 5, 24, 27, 32, 38, 44, 50 — SIN REGISTER
30, 34, 37, 38, 45, 50 — CYCLES OF INTEGRATION CONTROL
33, 35 ARE COMING FROM HARMONIC SELECTION CONTROL
39, 40, 47, 48 — DIGITAL OSCILLATOR CORRELATOR
28 — I.R.M. BOARD

NOTE

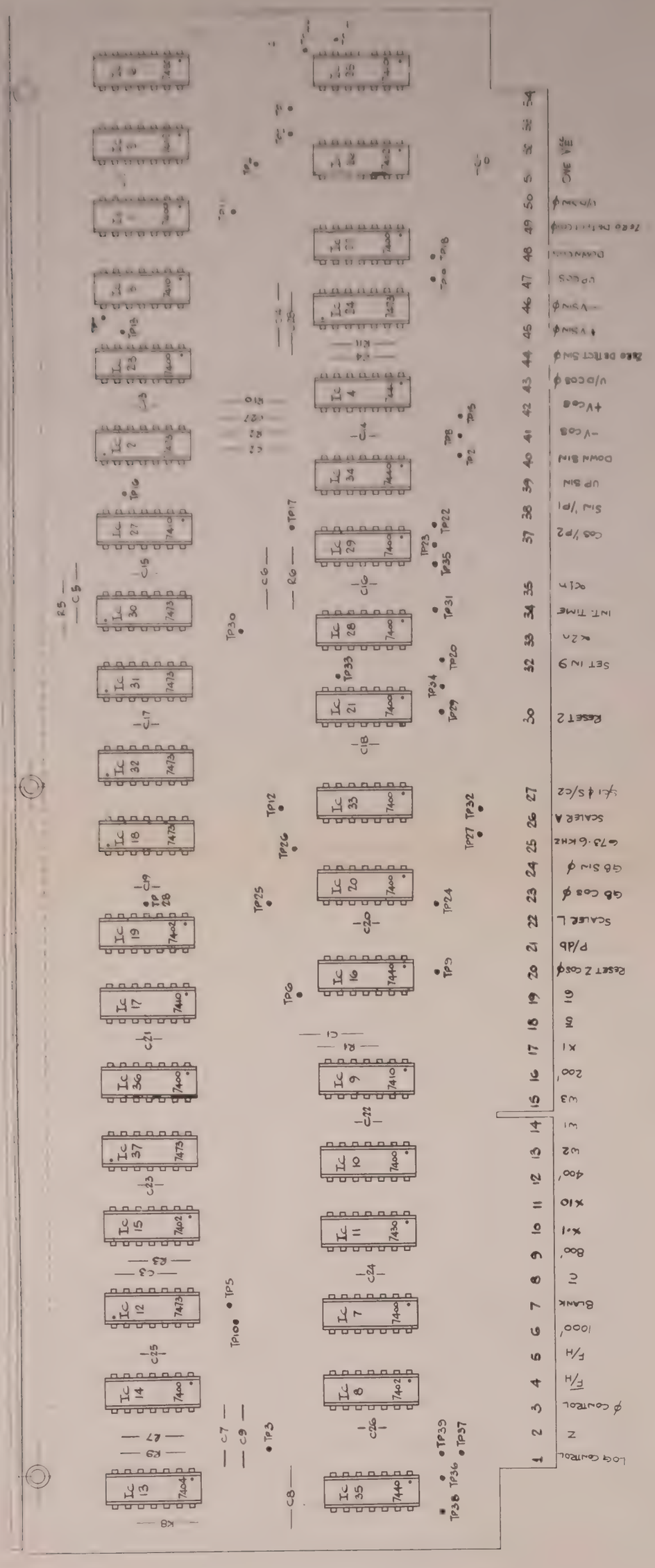
1 — POWER SUPPLY TO IC's. 1 — SN7473N (BISTABLES) +5VE PIN 4, OVE PIN 11
— ALL OTHER IC's. 1 +5VE PIN 14, OVE PIN 7

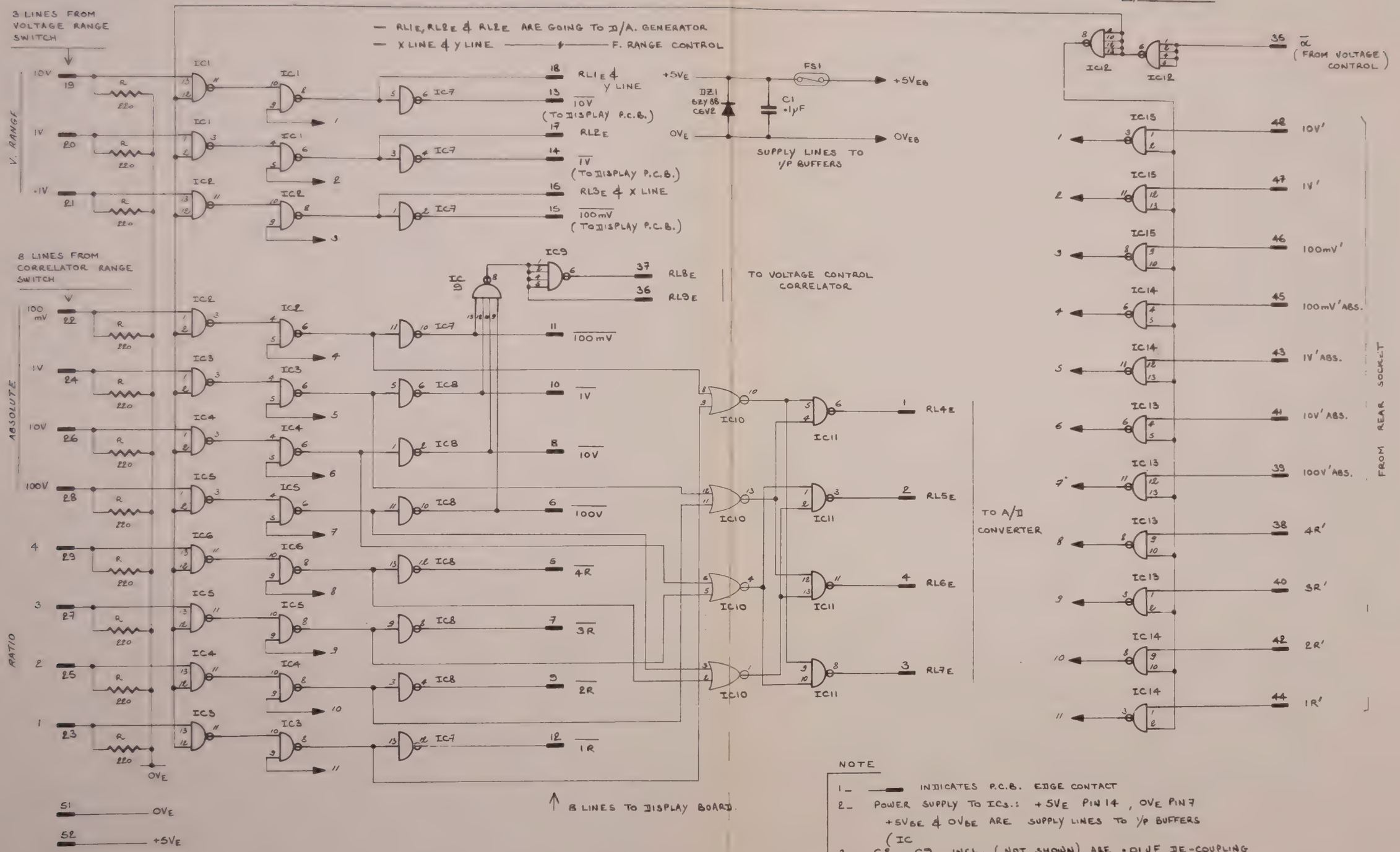
2 — C10 - C26 INCL. (NOT SHOWN) ARE .01 μF DECOUPLING CAPACITORS BETWEEN +5VE & OVE

3 — ⊖ & ⊖ INDICATES CONNECTION BETWEEN ORIGINAL P.C.B NO 2 ADDITIONAL P.C.B (WHICH CONSISTS OF IC 36, 37, 38, 39, R10, R11, C26 & C27

4 — INDICATES P.C.B EDGE CONTACT

TITLE: POLAR LOG CONTROL — CIRCUIT DIAGRAM (DS420 P)	JIG OR FIXTURE No.	PARTS LIST No. 30929	DRAWING No. E 32743
	SCALE	SERIES No. SM2001	

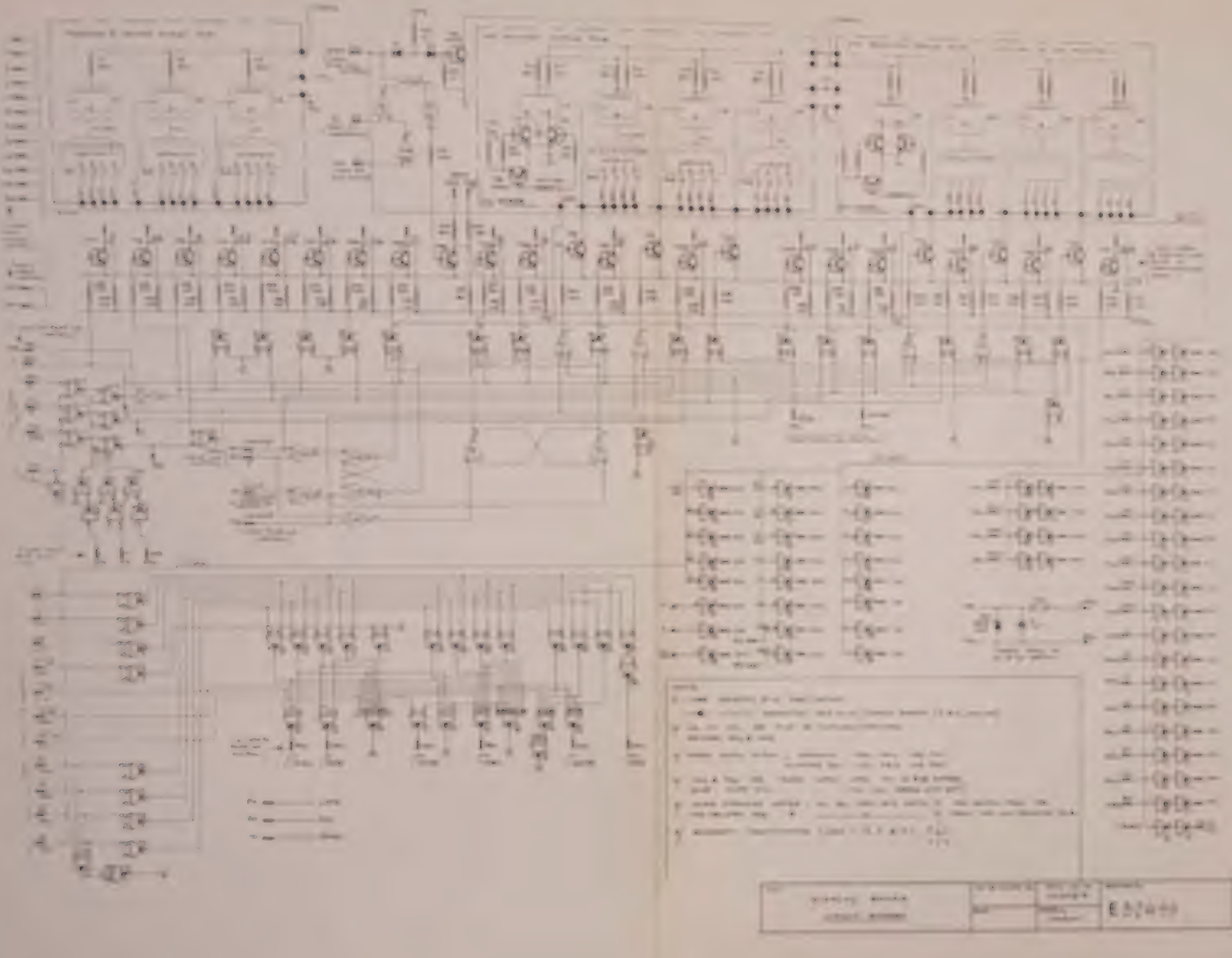

TITLE POLAR LOG CONVERSION CONTROL P.C.B. ASSY.
BOARD P
30929
SM2001
B30929
LOG CONTROL
ONE VEE
TP1
TP2
TP3
TP5
TP6
TP9
TP10
TP11
TP12
TP17
TP18
TP20
TP22
TP23
TP24
TP25
TP26
TP27
TP28
TP29
TP30
TP31
TP32
TP33
TP34
TP35
TP36
TP37
TP38
TP39

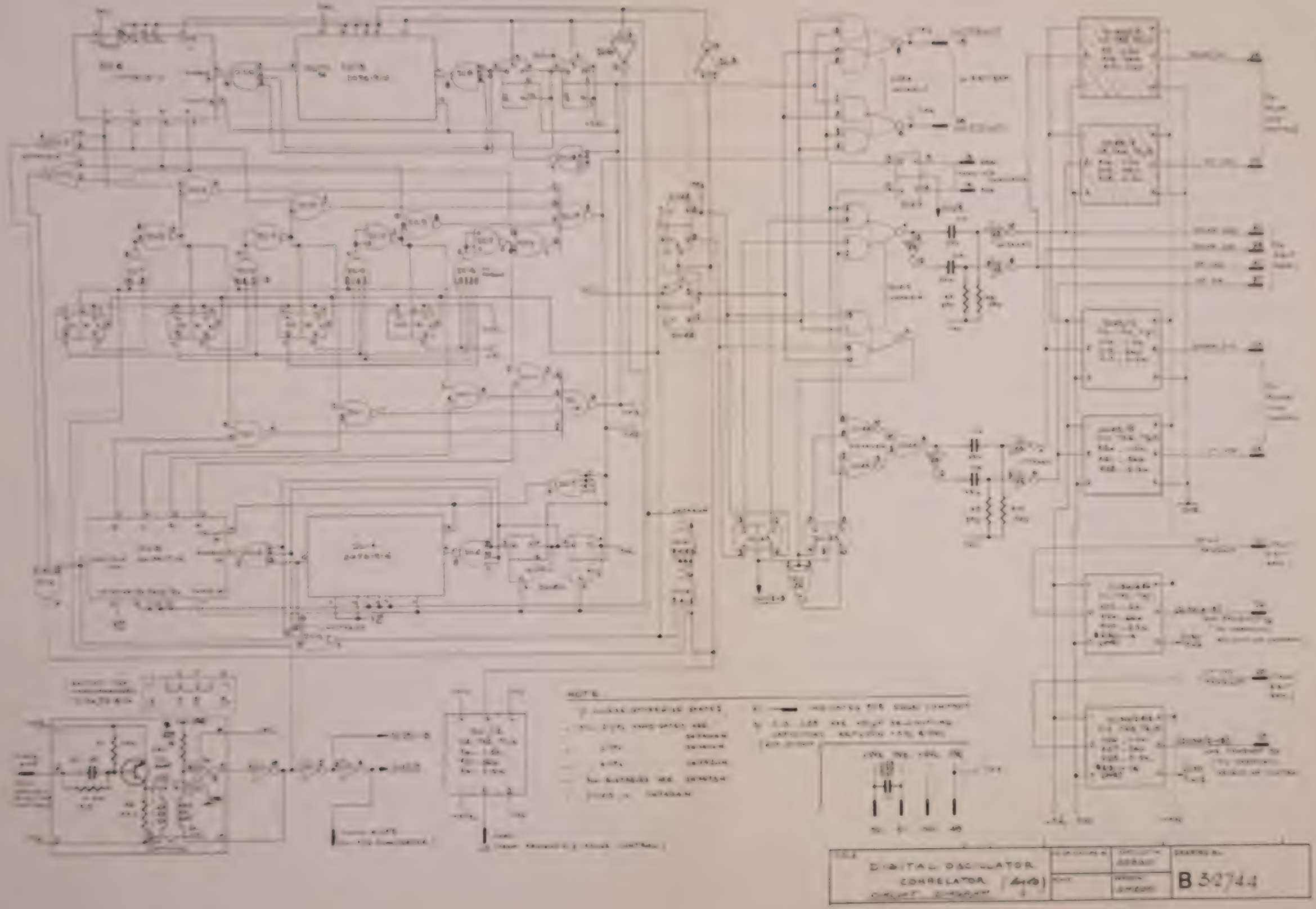


NOTE

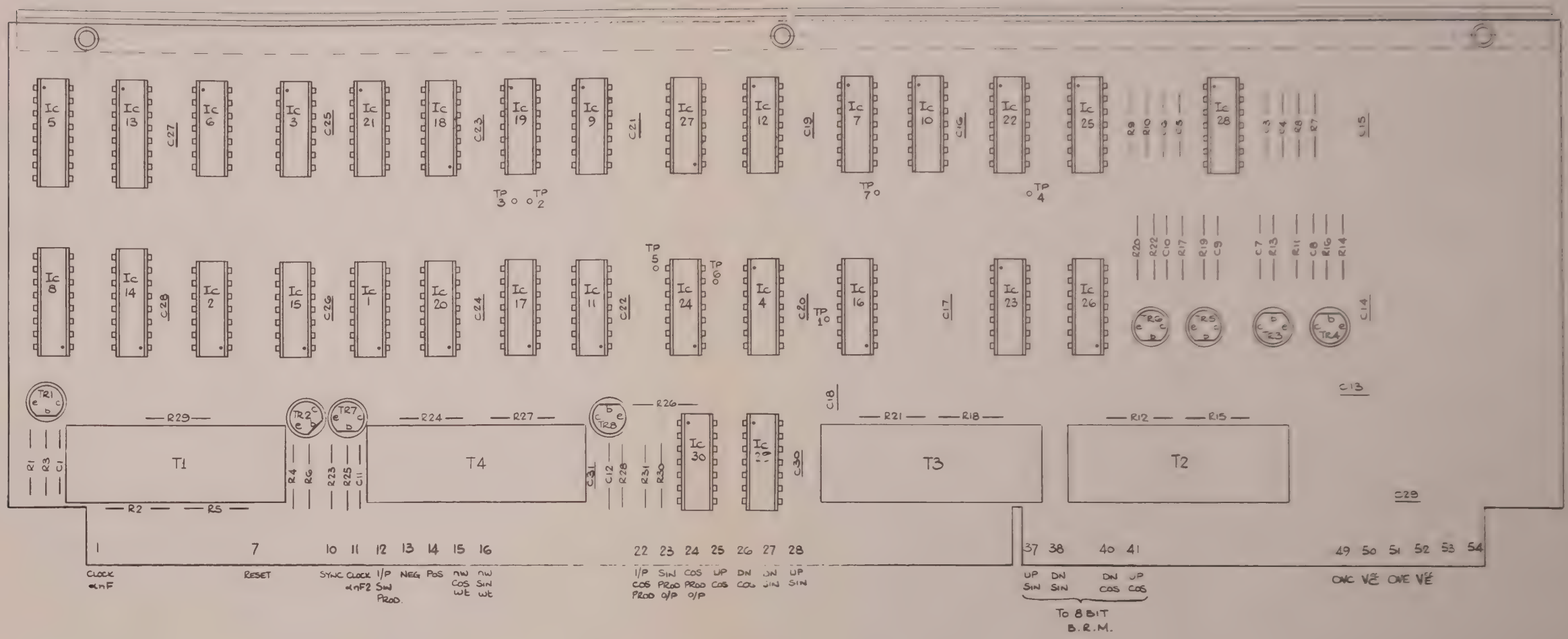
1. — INDICATES P.C.B. EDGE CONTACT
2. POWER SUPPLY TO ICs.: +5VE PIN 14, OVE PIN 7
   +5VBE & OVBE ARE SUPPLY LINES TO I/P BUFFERS
3. C2 – C9 (IC INCL.) (NOT SHOWN) ARE ·01μF DE-COUPLING CAPACITORS BETWEEN +5VE & OVE

TITLE	JIG OR FIXTURE No	PARTS LIST No	DRAWING No
AMPLITUDE & CORRELATOR RANGE CONTROL CIRCUIT DIAGRAM BOARD R		31486	B32677
	SCALE	SERIES No SM2001	

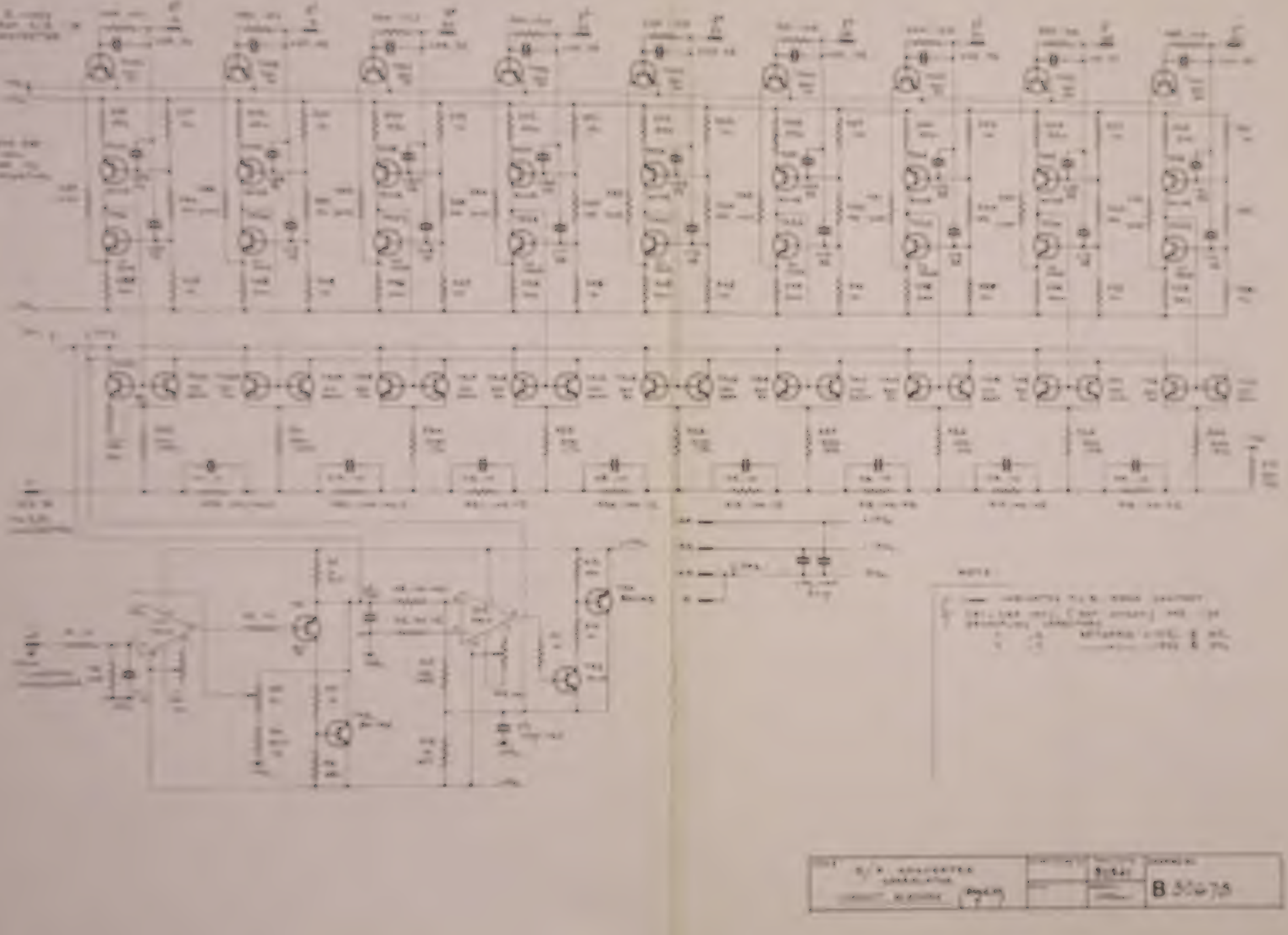



DIGITAL OSCILLATOR
CORRELATOR (4Ø)
B 32744

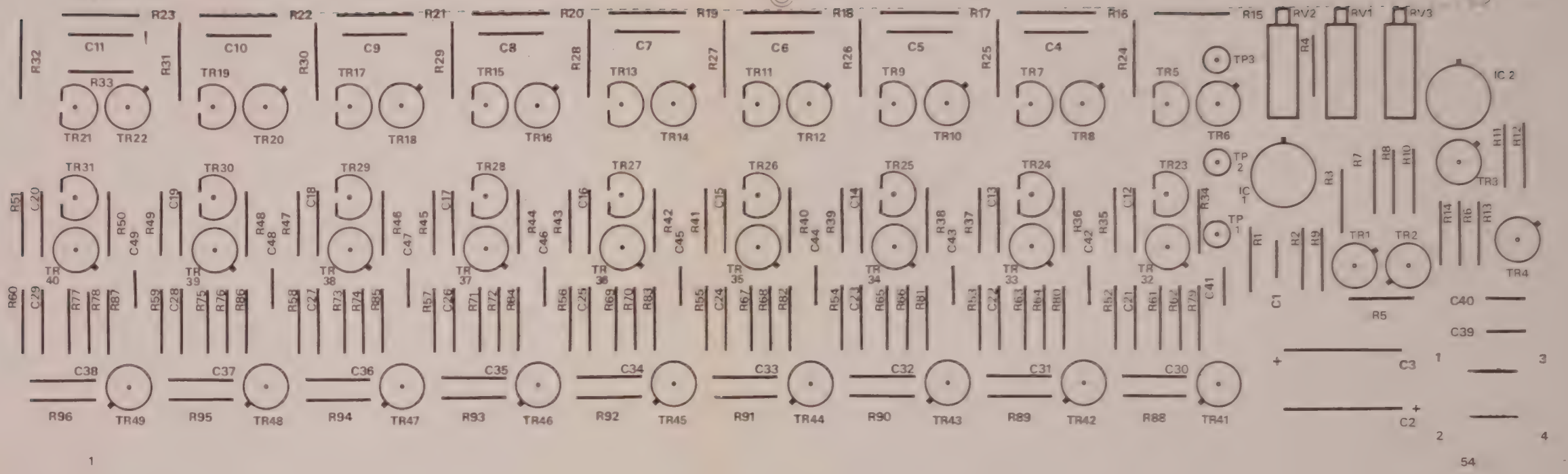
RIVET THIS SIDE
AFTER FITTING ITEM 16



TITLE DIGITAL OSCILLATOR-CORRELATOR P.C.B. ASSY. BOARD 5	CORE FIXTURE No.	PARTS LIST No. 30930	DRAWING No. B30930
	SCALE 2:1	SERIES No. SM 2001	



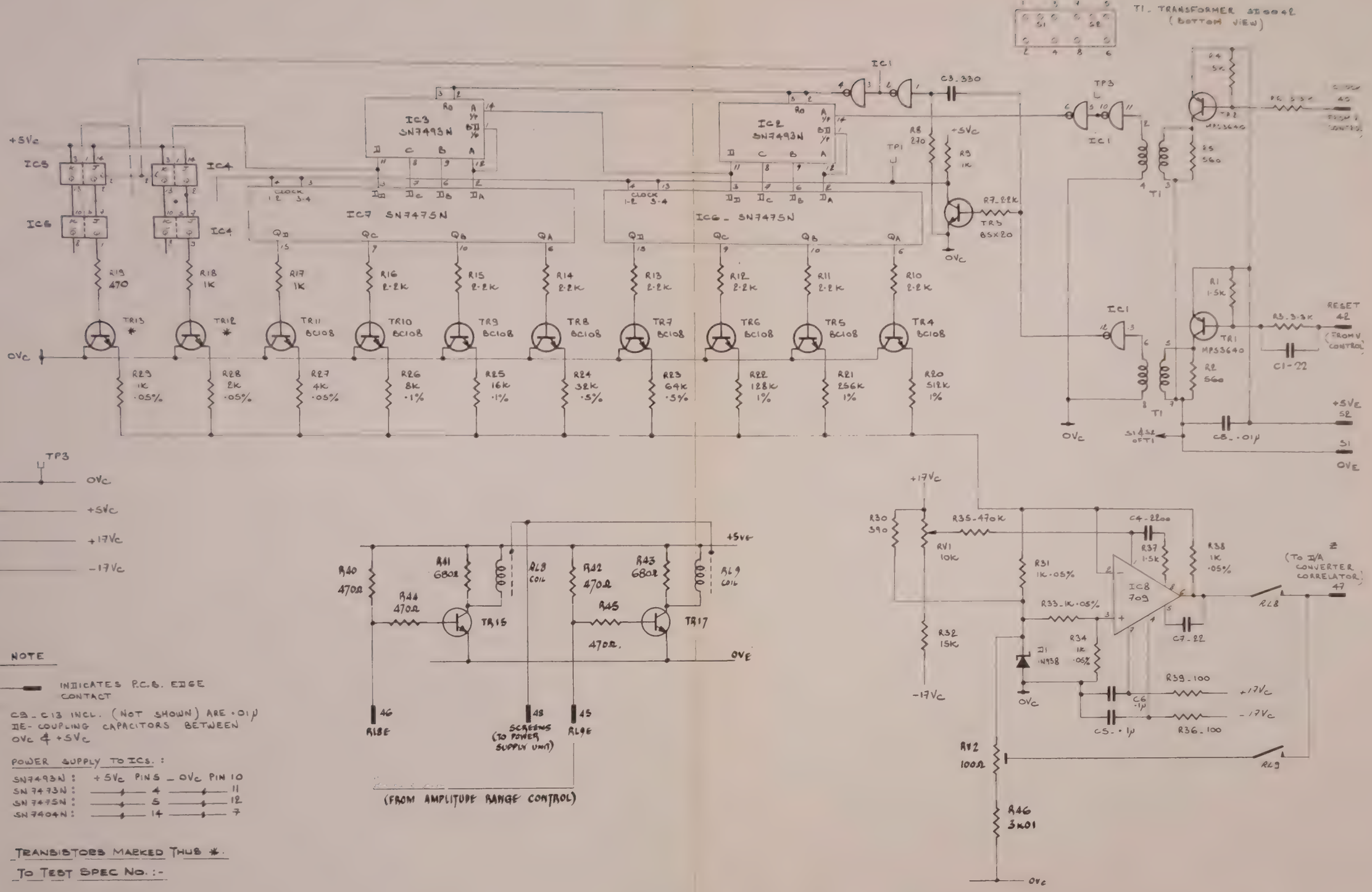
RIVET THIS SIDE
AFTER FITTING
ITEM 55



1

54

TITLE	JIG OR FIXTURE No	PARTS LIST No	DRAWING No
D.A CONVERTER (CORRELATOR) P.C.B ASS'Y (BOARD 1)		30931	B 30931
	SCALE 2:1	SERIES No SM 200	



NOTE

1/ —▬— INDICATES P.C.B. EDGE CONTACT

2/ C3 - C13 INCL. (NOT SHOWN) ARE ·01μ DE-COUPLING CAPACITORS BETWEEN 0Vc & +5Vc

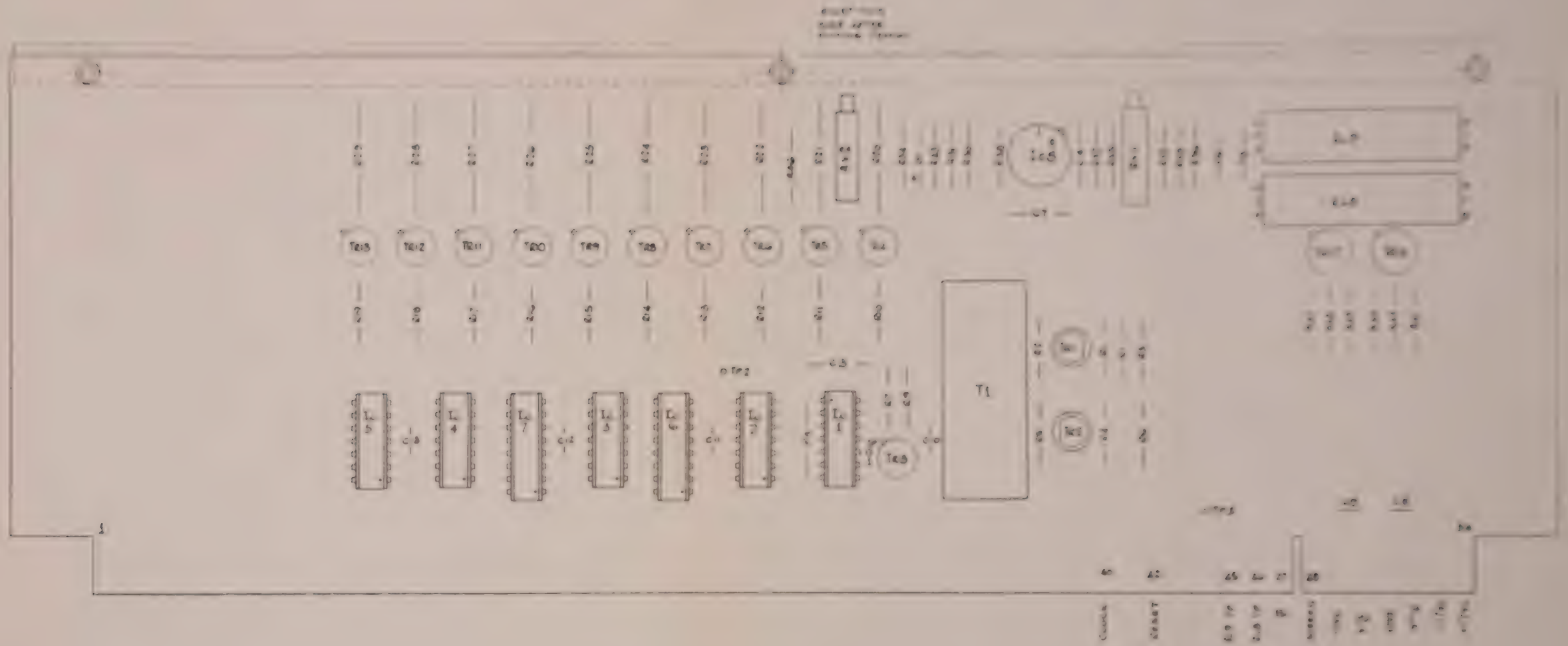
3/ POWER SUPPLY TO ICs. :

	+5Vc PINS	0Vc PIN 10
SN7493N :	4	11
SN7473N :	4	11
SN7475N :	5	12
SN7404N :	14	7

TRANSISTORS MARKED THUS *.

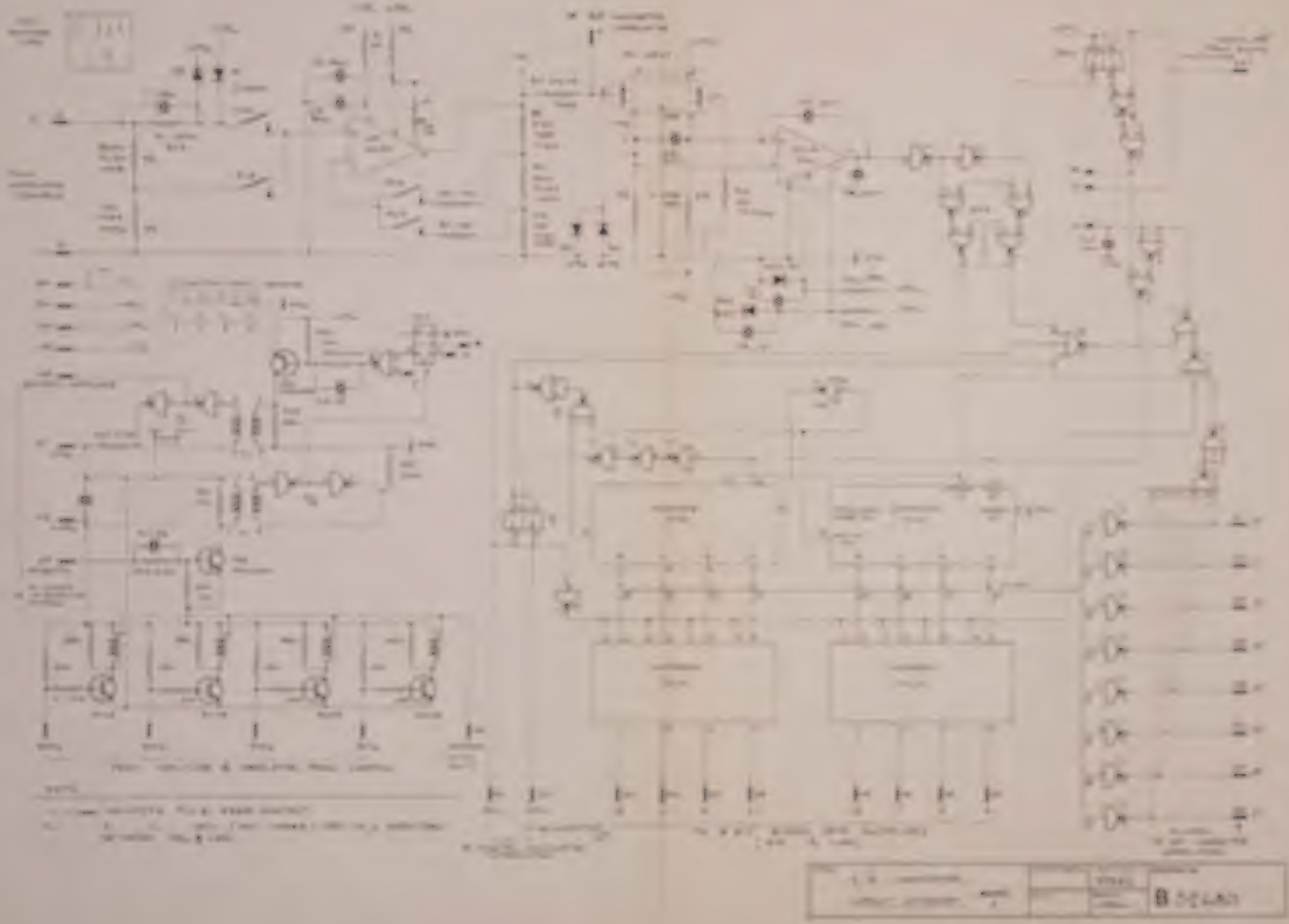
TO TEST SPEC NO. :-

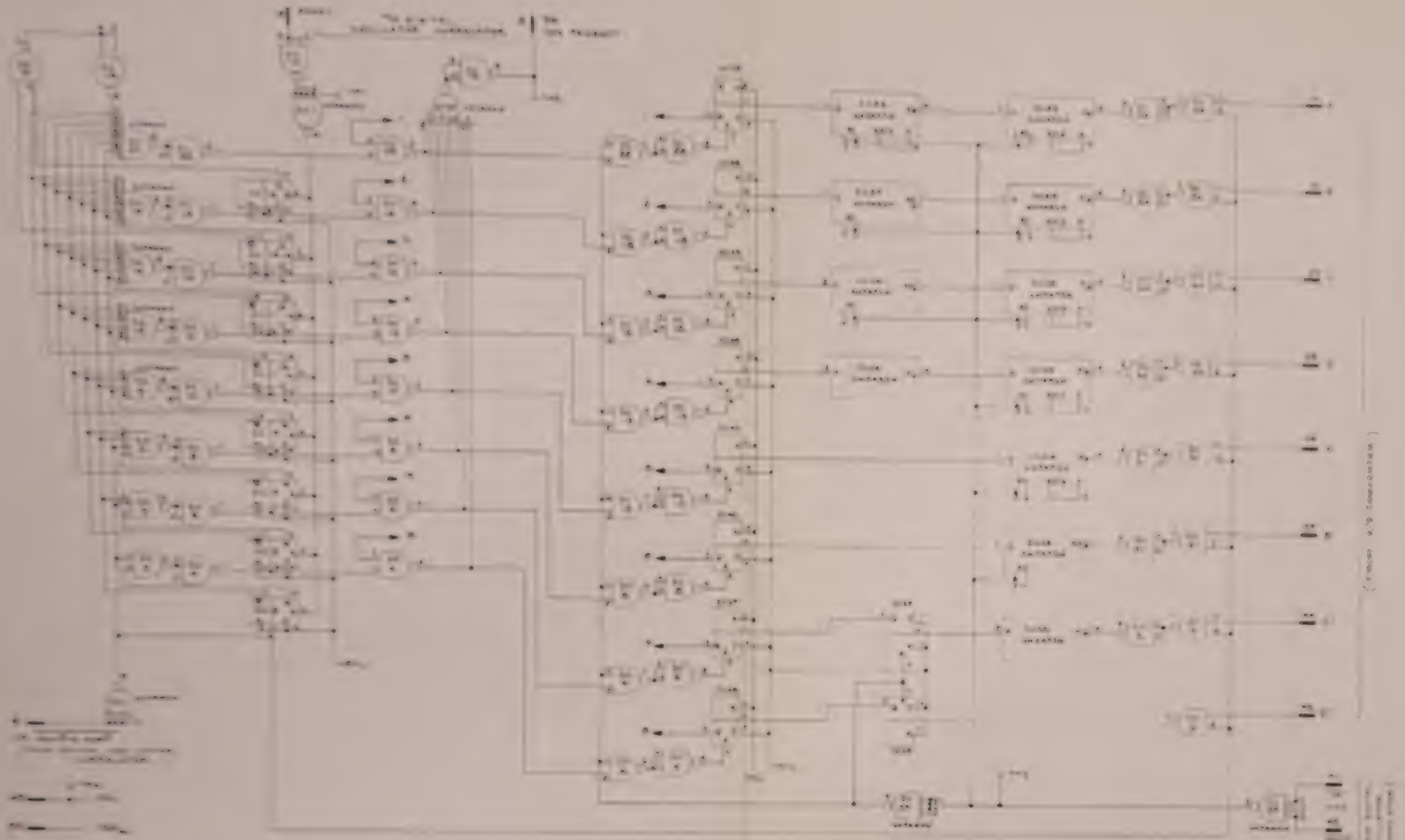
TITLE	VOLTAGE CONTROL CORRELATOR CIRCUIT DIAGRAM
JIG OR FIXTURE No	
PARTS LIST No	30933
DRAWING No	B 32679
SCALE	
SERIES No	SM2001



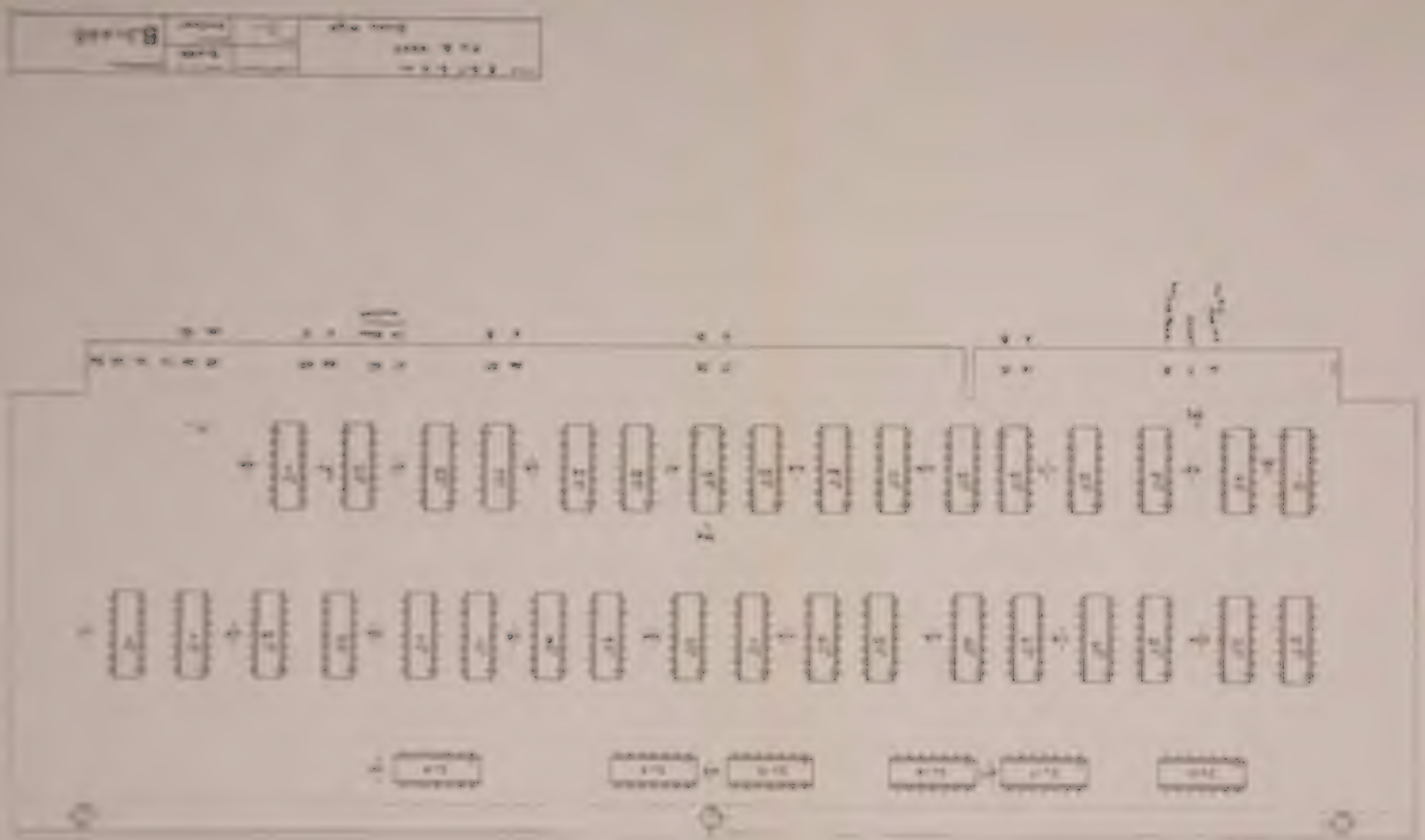
VOLTAGE CONTROL OSCILLATOR
PCB ASSY
BOARD U

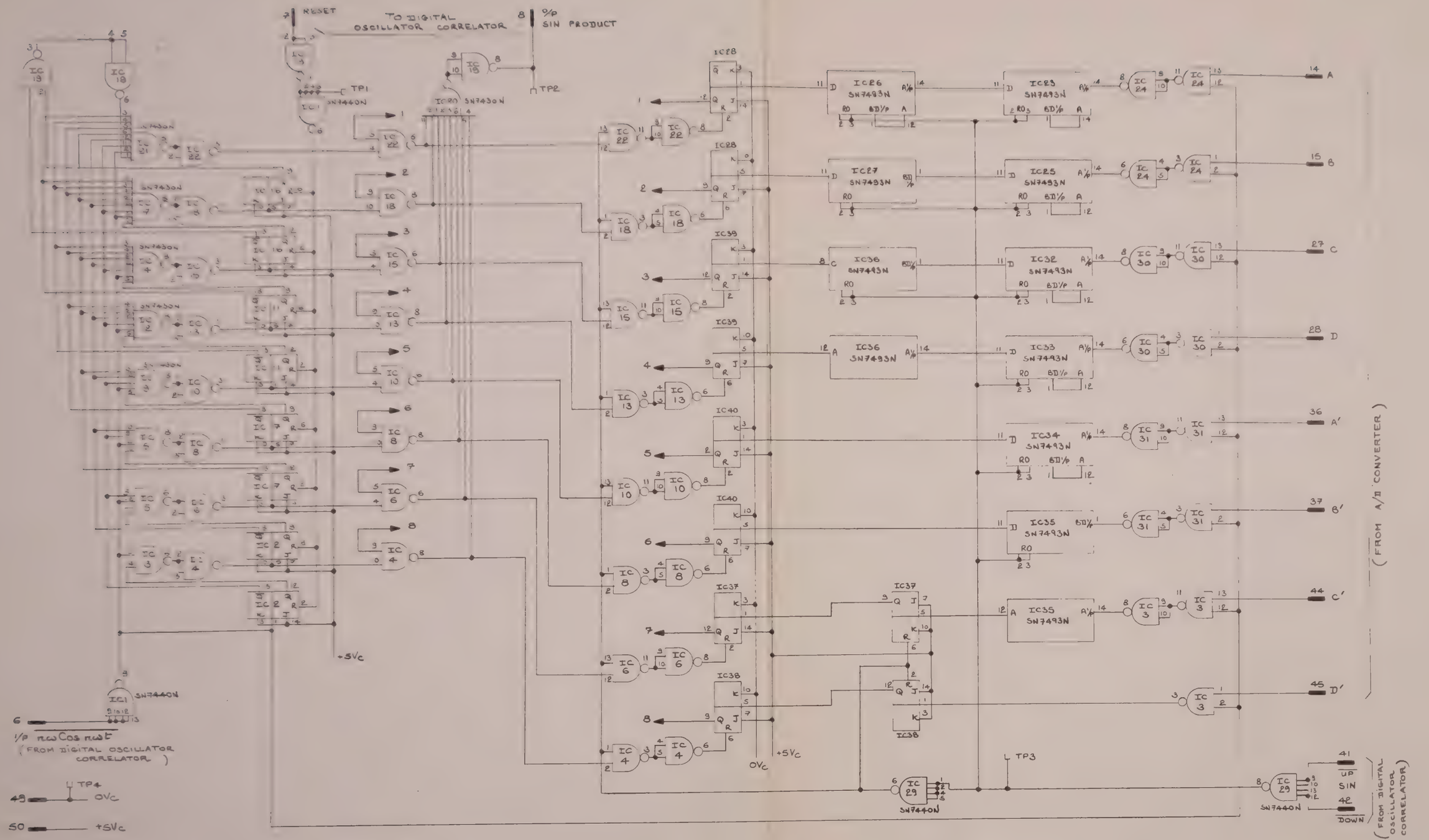
B 3683?





B 3.1489





NOTE

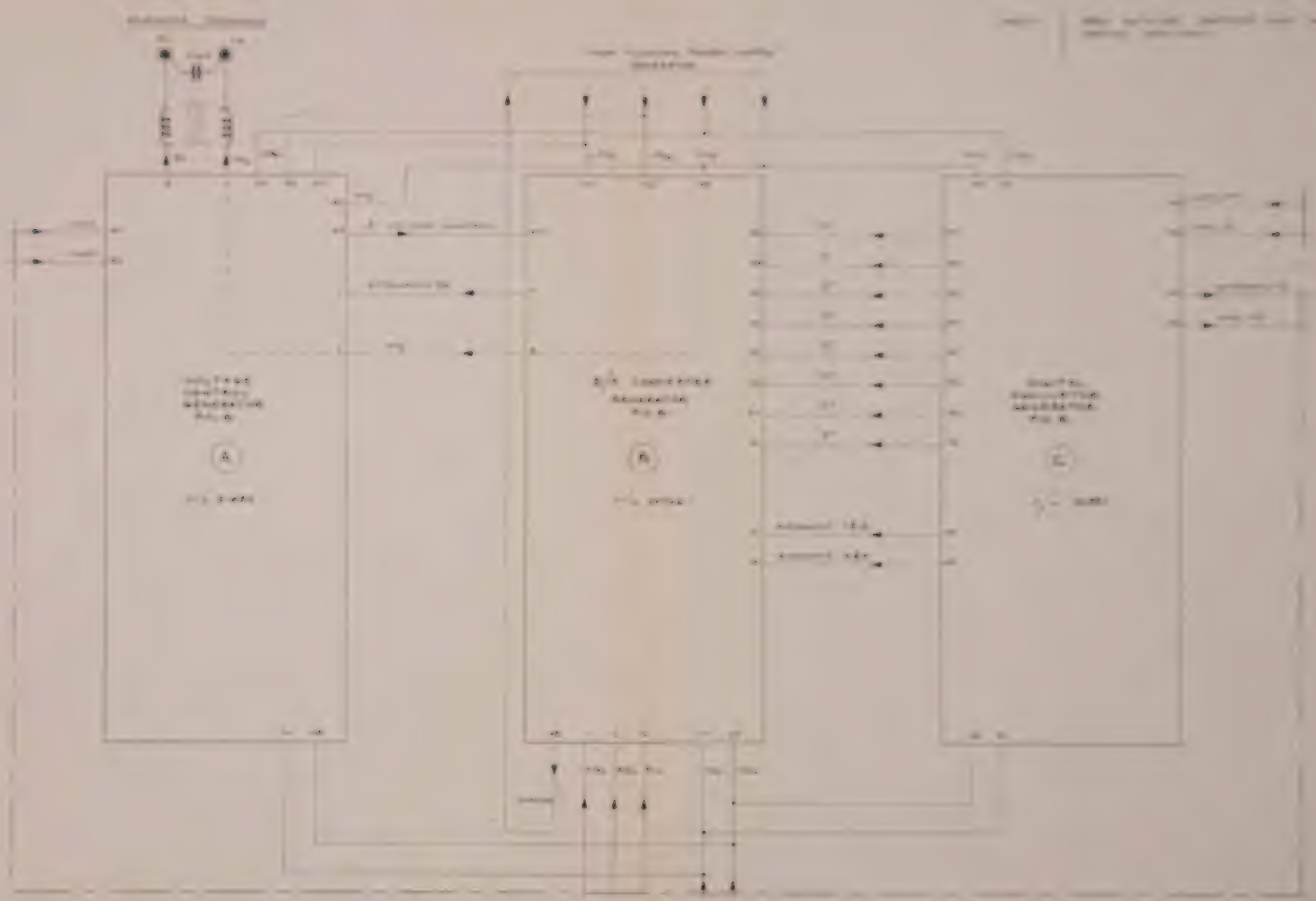
1/ ▬ INDICATES P.C.B. EDGE CONTACT

2/ C1 - C20 (NOT SHOWN HERE) ARE .01μF DE-COUPLING CAPACITORS BETWEEN 0Vc & +5Vc

POWER SUPPLY INTEGRATED CIRCUITS:

SN7493N - Vcc PIN 5, 0V PIN 10
SN7493N - Vcc PIN 4, 0V PIN 11 (Bistables)
ALL OTHER IC. - Vcc PIN 14, 0V PIN 7

TITLE	JIG OR FIXTURE No	PARTS LIST No	DRAWING No
8 BIT BINARY RATE MULTIPLIER (SIN) CIRCUIT DIAGRAM X		31488	B 32691
	SCALE	SERIES No SM2001	



NOTE

1. ... INDICATES WIRING POINT ON MODULES P.C.B.
2. THE OPTIONAL HARMONIC LINES & FILTER OUTPUT CONNECTIONS ARE NOT SHOWN ON THIS DRAWING (...)

TO HRON SOURCE ON FRONT PANEL

DISPLAY P.C.B. P/L 30830

COA REGISTER DISPLAY P.C.B. P/L 30826

SIN REGISTER DISPLAY P.C.B. P/L 30826

COA REGISTER P.C.B. P/L 30827 (M)

SIN REGISTER P.C.B. P/L 30828 (N)

POLAR LOG CONTROL P.C.B. P/L 30830 (P)

CYCLES OF INTEGRATION P/L 30829

OPTIONAL BOARDS

9 LINES TO/FROM GENERATOR SECTION

18 LINES TO/FROM CORRELATOR SECTION

SIN PRODUCT

COS PRODUCT

CLOCK ENP

CLOCK

TRANSFER & RESET

FIND ME

P LINES

11 LINES

HARMONIC SELECTION CONTROL P.C.B. P/L 30825 (L)

CLOCK ×F

CLOCK ×OF

AMPLITUDE CONTROL P.C.B. P/L 31486 (R)

R.O.E

R.S.E

R.O.E

R.T.E

R.B.E

R.O.E

'MEASURE' PUSH-BUTTON & OVERLOAD ME LATCH

TO CYCLES OF INTEGRATION CONTROL P.C.B.

TO F. RANGE CONTROL P.C.B.

F/8a

F/8b

F/8c

F/8d

FREQUENCY RANGE SWITCHES

VOLTAGE RANGE SWITCH

CORRELATOR RANGE SWITCH

RATIO

ABSOLUTE

+5V

To DISPLAY P.C.B.

E, 32b

B, 32b

B/4b, 32b

HARMONIC SWITCH

DISPLAY SWITCHES

RUN

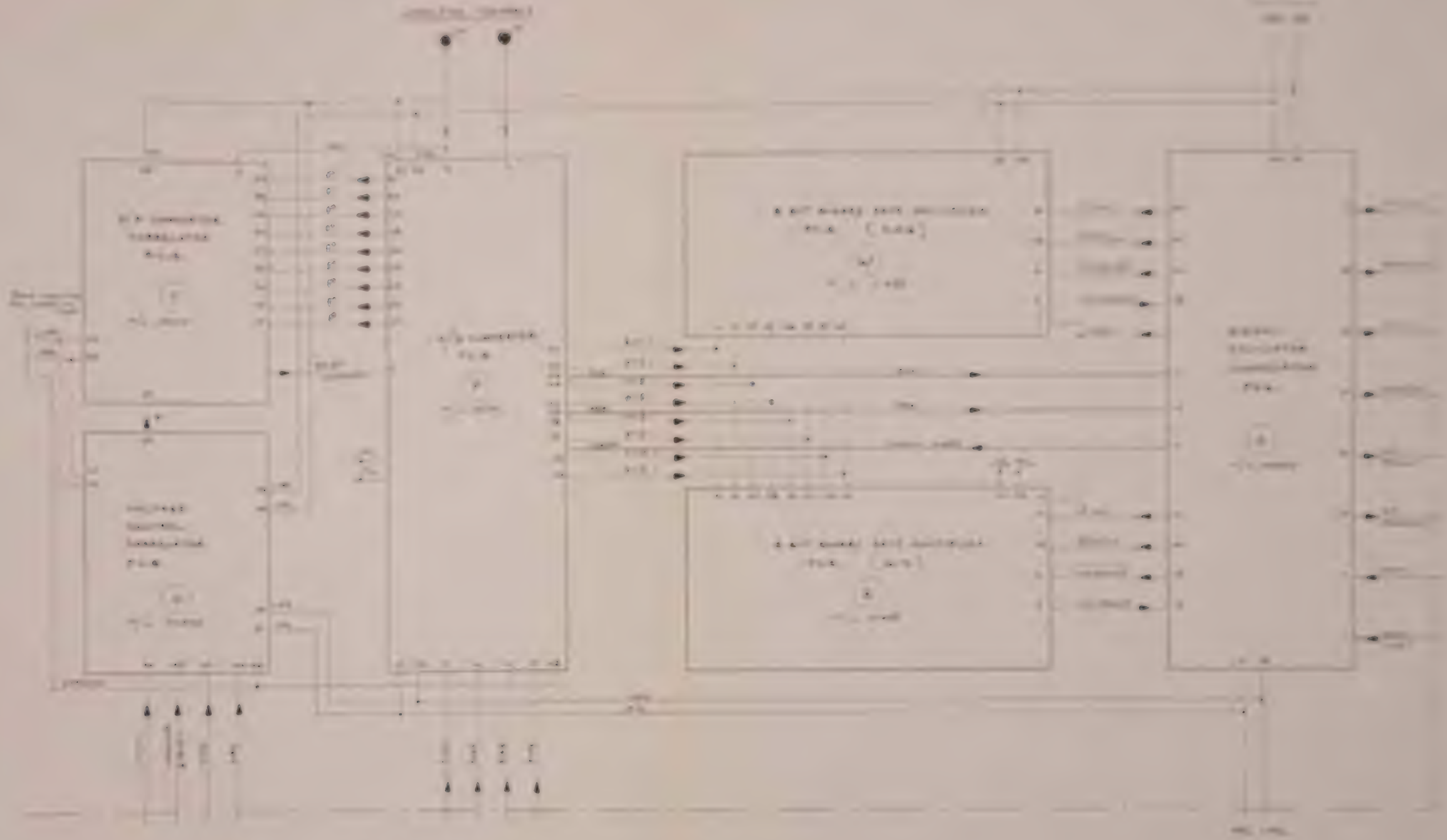
STOP 0°

STOP 30°

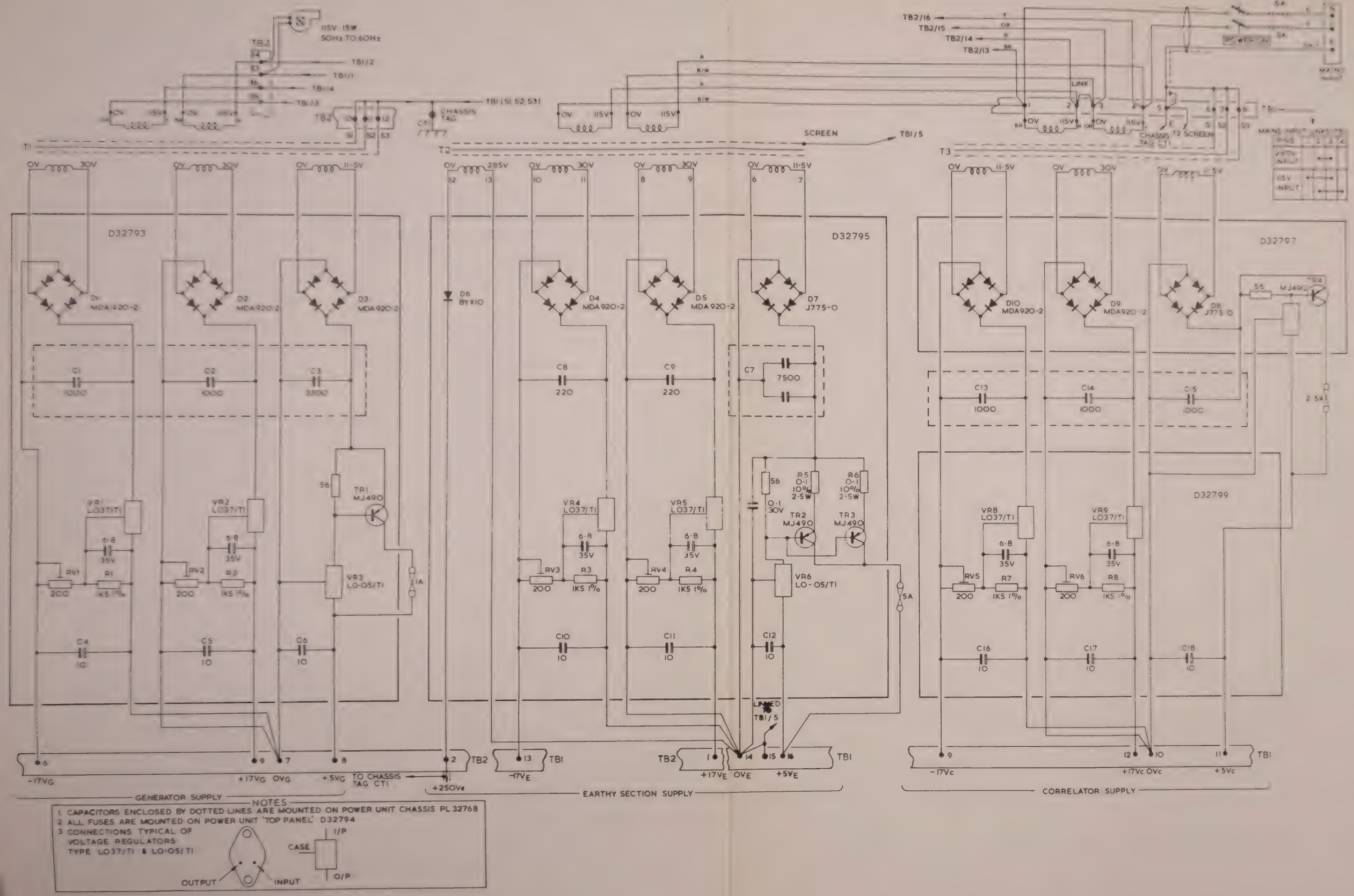
STOP 80°

STOP 120°

TITLE	JIG OR FIXTURE No	PARTS LIST No	DRAWING No
EARTHY SECTION INTERCONNECTION BLOCK DIAGRAM.	SCALE	SERIES No	E 32a30



B57648



NOTES

1. CAPACITORS ENCLOSED BY DOTTED LINES ARE MOUNTED ON POWER UNIT CHASSIS PL32768
2. ALL FUSES ARE MOUNTED ON POWER UNIT 'TOP PANEL' D32794
3. CONNECTIONS TYPICAL OF VOLTAGE REGULATORS TYPE LO37/TI & LO-05/TI

SUPPLEMENT NO. 2002

Issue 2, October 1973.

REFERENCE SYNCHRONISER SM 2002

List of Contents

1. Specification
2. General Information
3. Installation
4. Operating Instructions
5. Application Notes
6. Theory of Operation
7. Circuit Description
8. Checks and Adjustments

Circuit Diagram

Boards Component Layout

REFERENCE SYNCHRONISER SM 2002

1. SPECIFICATION

Items of Equipment	$\frac{1}{T}$ Generator Board E 31494 Balance Control Board E 31495
Frequency Range of Input:	0.001 Hz to 999 Hz
Amplitude of Input:	150 mV r.m.s. to 230 V r.m.s.
Operating Temperature Range:	0^{o}C to $+50^{o}$C

2. GENERAL INFORMATION

2.1. This unit consists of two plug-in printed circuit boards which can be purchased separately.
It is used where the system-under-test cannot be excited by the generator output but requires some other source, (as with a mechanical prime mover). A synchronisation signal is provided by the source and taken to rear panel inputs on the frequency response analyser. External synchronisation mode is selected by the front-panel, illuminated, latching push-button and the unit then computes and displays the input frequency in two cycles of the input signal.

2.2. Ratio measurements in the 'ext. sync.' mode using the front panel MEASUREMENT selector (see ***page 3-6 of the instruction manual***), cannot be made. However, a form of ratio measurement can be made using an externally connected switch applying, alternately, the external reference signal and the return signal from the system-under-test to the correlator section (see ***Para. 4.3 of this supplement***).

3. INSTALLATION

3.1. To fit the SM 2002 p.c. boards to the SM 2001, proceed as follows:

(a) Remove the top cover

(b) Remove the two board clamps (if fitted)

(c) Insert the $\frac{1}{T}$ Generator Board (E 31494) into the eighth socket (SKT H) from the left (as viewed from the front) in the main board box.

(d) Insert the Balance Control Board (E 31495) into the ninth socket (SKT J) from the left (as viewed from the front) in the main board box

(e) Refit the board clamps and the top cover

4. OPERATING INSTRUCTIONS

4.1. With the SM 2002 Reference Synchroniser fitted, connect an external reference oscillator between the EXT SYNC INPUT terminal and the earth terminal on the rear panel. The signal must be within the frequency range and amplitude limits stated in Para. 1, Specification. The signal must alternate between positive and negative values, through OV and ideally, the positive going transition through OV should occur at the zero degree phase point for optimum accuracy (see ***Para. 5 Application Notes.***)

(a) Switch on the SM 2001

(b) Depress the SET F push-button

(c) Depress the EXT SYNC. push-button

4.2. The Generator display now indicates the input frequency of the external reference oscillator, plus a small amount, after 2 cycles have occurred.

4.3. All measurments can now be made as for normal operation except RATIO (see ***SM 2001 Instruction Manual, Section 3, Para. 7.2,*** but deleting reference to the Generator Section). However, ratios measurements can be made by use of an externally connected switch (SW1) as shown in Fig. 1.

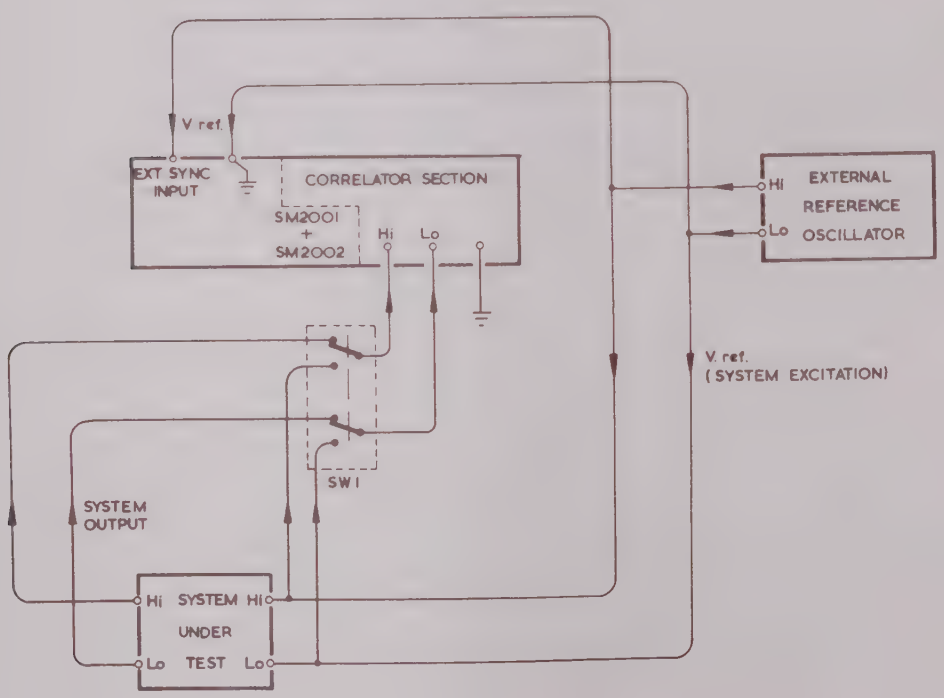


FIG.1. METHOD OF TAKING RATIO MEASUREMENTS

5. APPLICATION NOTES

5.1 In order to be able to make full use of the lower limits of the frequency range (0.001 Hz) the EXT SYNC input has to be directly coupled. Therefore, if d.c. is present on the input, the external sync system will not work unless the superimposed a.c. component takes the input level through 0V to a negative value (see fig.2A). If the a.c. component is alternating centrally about the zero base line, no phase error will be evident (a = b). However, if the base line is moved (for example, a d.c. bias is added), the a.c. component no longer alternates equidistantly (a does not equal b), and phase errors will result (fig.2B).

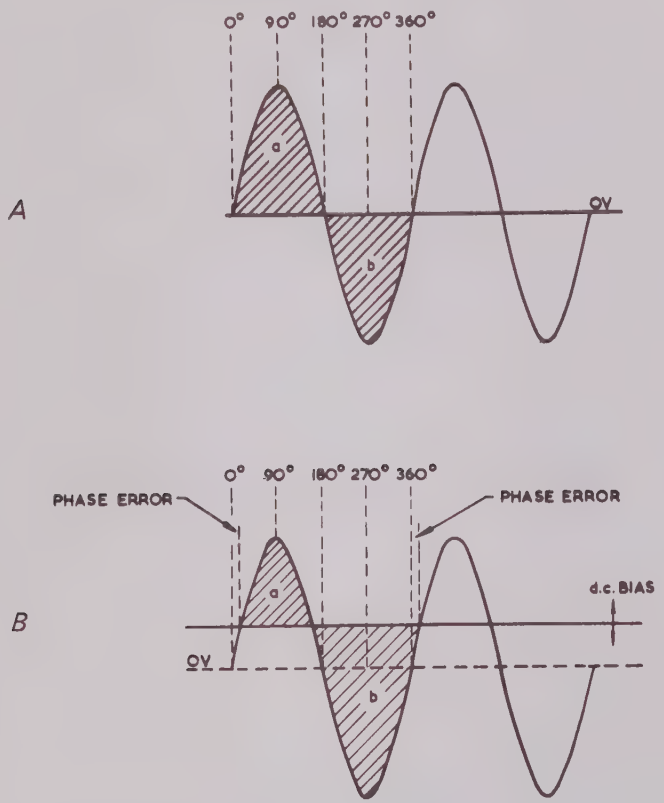


FIG.2. PHASE ERRORS CAUSED BY SHIFTING D.C. BASELINE

5.2 Phase errors can be measured by connecting the output of the external signal source to the EXT SYNC INPUT terminals and the CORRELATOR INPUT terminal, with EXT SYNC selected (see *SM 2001 Instruction Manual, Section 3, Para. 6.2(b) Correlator Displays).*

6. THEORY OF OPERATION

6.1 Consider the block diagram below:-

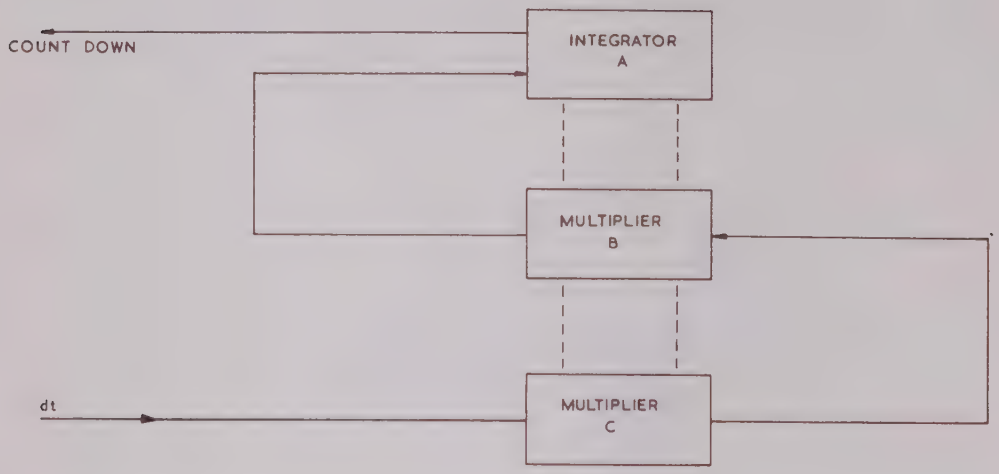


FIG.3. BLOCK DIAGRAM

The output of multiplier C will be,

$$C = Adt$$

and the output of multiplier B will therefore be,

$$B = A^2dt$$

This output is integrated downwards so that,

$$A = -\int A^2dt$$

$$\text{therefore } dA = -A^2dt$$

$$-\frac{dA}{A^2} = dt$$

the solution of which is $t = \frac{1}{A}$ or $A = \frac{1}{t}$

and $\frac{1}{t} = F$ (frequency).

6.2 To implement this function requires a starting frequency of infinity but if the start is set at 999 Hz and also delayed for 1ms the result is correct, after the 1ms delay. This is how we compute the synchronizing frequency in the SM2002.

7. CIRCUIT DESCRIPTION

7.1 Introduction

7.1.1 The SM2002 contains the following functions:-

(a) $\frac{1}{t}$ generation

(b) Balance control

(c) Reference input squaring

7.1.2 The block diagram below shows how the different functions are linked together, and to the SM2001.

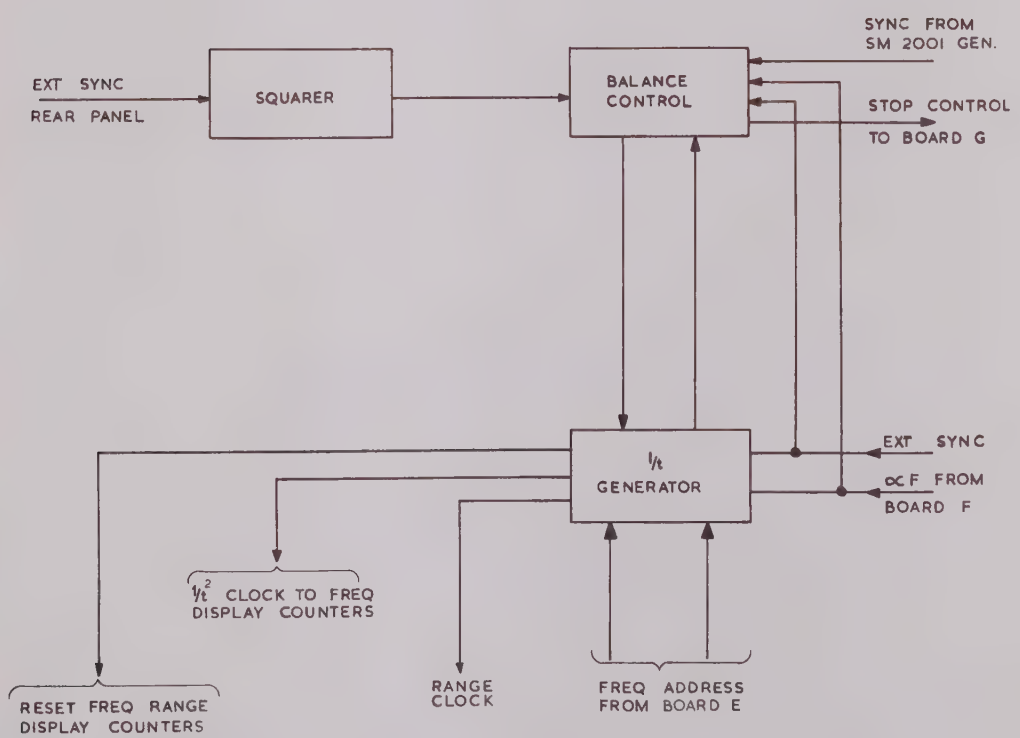


FIG.4. BLOCK SCHEMATIC OF SM2002.

7.2 $\frac{1}{t}$ Generation

7.2.1 The 1/t function is generated as shown in the theory section but only the multiplier B is on board H, the 1/t generator. The integrator is the display frequency counter on board E and the multiplier C is the frequency multiplier on board G.

7.2.2 A further addition is that, to obtain highest accuracy, the integrator value is reset to 999 when the counter goes below 100 and the range is changed down so that an extra divider is added between multiplier C and multiplier B which is on board F.

7.2.3 The multiplier is the same circuit that is used on board G, which is described in the SM2001 circuit description. The multiplier output is then used to drive the following circuits, shown in block diagram form in fig.5.

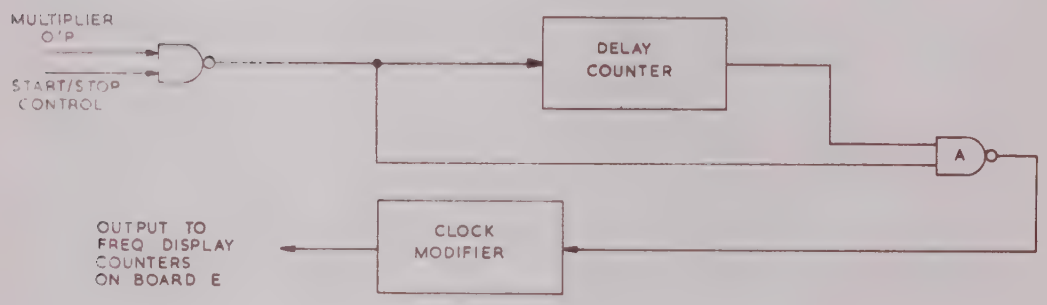


FIG.5

7.2.4 When the start/stop line goes high (determined by the balance control circuit and the reference frequency zero-crossing edge) the multiplier output is fed into the delay counter which then enables gate A after the 1ms delay discussed previously. The output from gate A goes into the clock modifier circuit (which actually uses many of the components in the delay counter, but is shown separately for simplicity). The clock modifier is a multiplier with a fixed address which adjusts the pulse rate output to be in the correct units for an accurate 1/t generation.

7.2.5 The clock modifier includes gating to detect when the display frequency goes below 230 (independent of range) when more pulses are allowed through, i.e. the slope of the curve is altered. This is necessary because there is a limitation on the accuracy of the curve using this method (far greater accuracy can be achieved by 1/t generation but not in this implementation).

A further addition is that an extra pulse is generated at the end of every other 1/t generation (bistable IC37/9 triggered from 1/t bistable). Again this is to improve performance at the low end of each range.

7.2.6 The 1/t function is initiated by a control line from the balance control board and there is a loop between the two boards controlling the whole operation. This loop is shown in detail below.

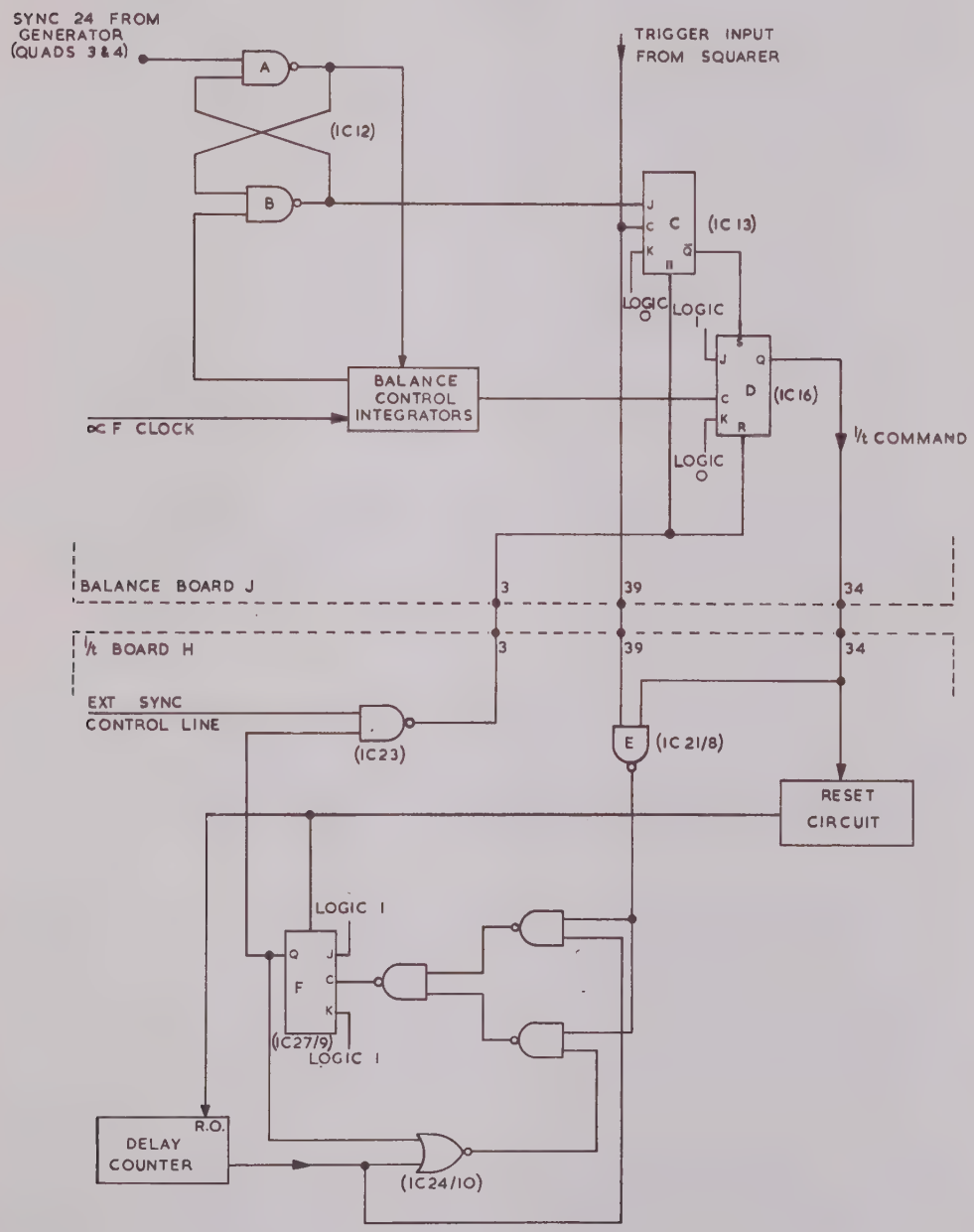


FIG. 6. 1/t CONTROL LOOP

7.2.7 The 1/t command can be initiated from two sources:

(a) *R-S Latch Comprising Gates A & B and the Trigger Input.* During the balance control period (discussed in the next section) gate B output is at logic 0 and if the trigger input occurs during this period bistable C will not change state - this being the correct mode of operation. However if the trigger input occurs before the sync pulse from the generator section gate B output will be at logic 1 and bistable C will toggle to logic 1 output, the Q output going to logic 0 and setting bistable D to logic 1 on 1/t command line.

(b) *Balance Control Integrator Section.* If the trigger input occurs later than the period allowed by this circuit the output to the clock input of bistable D will go low toggling bistable D causing the 1/t command line to go high.

7.2.8 The 1/t command line resets the multipliers and counters associated with the 1/t generator and enables gate E. The first trigger input after the gate is enabled will toggle bistable F, and if the next trigger pulse occurs after the 1ms delay this next trigger pulse will toggle bistable F back again. Thus the output of bistable F will be high between trigger pulses during which the 1/t generation is carried out.

7.2.9 When bistable F output returns to 0, bistables C and D are reset and the 1/t command is removed. If the system has acquired the correct frequency the SM2001 can now be used to make measurements on the external signal. The system is inhibited when the EXT SYNC push button is released.

7.3 Balance Control.

7.3.1 The purpose of the balance control circuit is to position the internal generator sinewave (which has a shorter period than the reference signal by design) such that the 180 degrees points of the two signals coincide. The errors caused by the difference in frequency will then be minimised.

7.3.2 When the system is locked on, the balance control works as follows. The sync pulse from the generator (Sync.) sets the R-S flip-flop made up of gates A and B, the output of gate A being used to stop the digital oscillator at 360 degrees. The output from gate B now enables gate G, and αF pulses are counted up in counter J from the value held in it until the trigger input derived from the zero-crossing of the reference input is generated. This transfers half the value of the counter J into counter K. This removes the zero-detect inhibit on gate H which allows αF pulses into counter which counts down to zero. This is detected and this resets the R-S (gates A and B) and inhibits gate H. Resetting the R-S inhibits pulses into counter J and allows the internal digital oscillator to start by removing the inhibit on the αF pulses (board F).

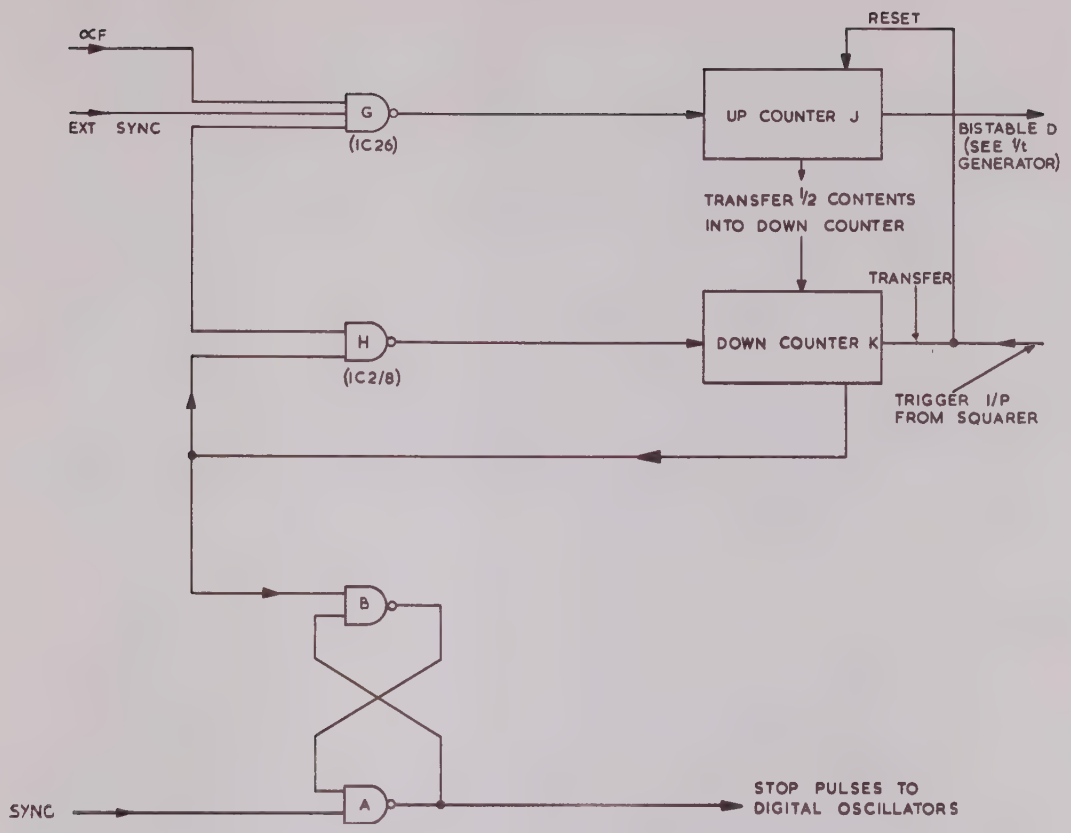


FIG. 7. BLOCK SCHEMATIC OF BALANCE CONTROL CIRCUIT

7.3.3 *Theory of Operation.* When the internal digital oscillator reaches 360 degrees, let the number held in counter J be x. If y more pulses are counted-in until the trigger pulse occurs, the counter J holds x+y. (x+y)÷2 is transferred into counter K which counts down to zero, thus (x+y)÷2 pulses are fed into counters J and K.

When counter K reaches 0, counter J contains (x+y)÷2, which it holds during one cycle of the internal digital oscillator.

If the relationship between the two frequencies is the same at the next balance period, counter J starts from (x+y)÷2 and will have (x+y)÷2 pulses counted-in until the trigger occurs. Thus the digital oscillator is balanced inside the period of the reference signal.

Fig.8 shows that there are (x+y) pulses between the stop and start of the digital oscillator with (x+y)÷2 between the 360 degrees point and the trigger input and (x+y)÷2 between the trigger input and the 0 degree start of the digital oscillator.

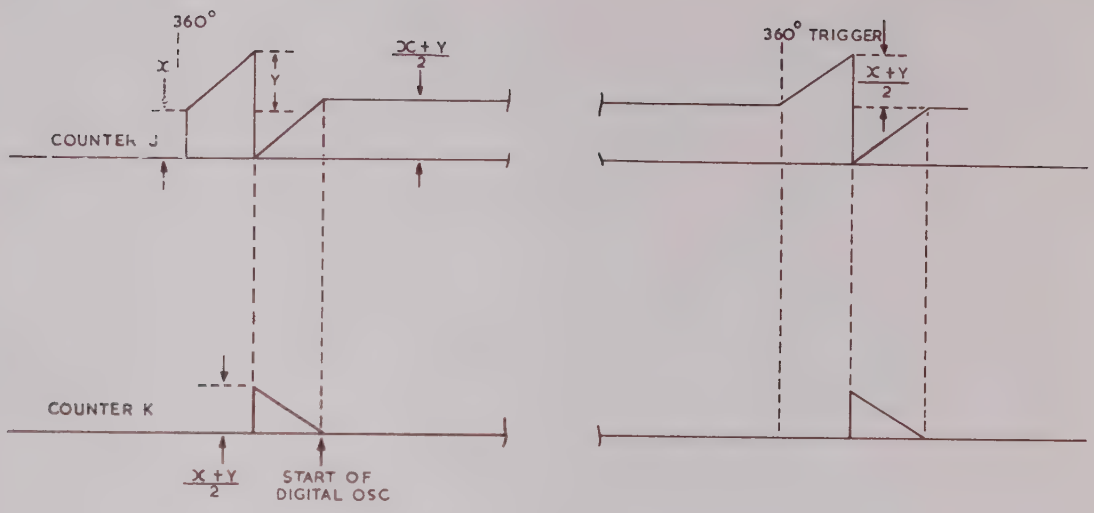


FIG. 8. ANALOGUE REPRESENTATION OF COUNTER CONTENTS

The counter J can overflow if the difference between the two frequencies is too large to give accurate measurements and this overflow triggers bistable D and initiates 1/t generation.

7.4 Reference Input Squarer.

7.4.1 This is a fairly conventional circuit using a dual f.e.t. input (TR1) for the high input impedance required. This is followed by transistor differential stage formed by TR3 and TR4 driving a comparator IC18. A small amount of positive feedback is used (R14,C7) to speed-up the output transition which is necessary as the lowest frequency that the system will lock to is less than 0.001Hz.

7.4.2 The potentiometers RV1 and RV2, are used to adjust for one transition of the output of the comparator to occur at the positive zero-crossing of the input signal (the 0 degree point of a sine wave).

8. CHECKS AND ADJUSTMENTS

8.1 Test Equipment Required.

(a) Frequency Response Analyser SM2001. This must be the parent unit into which the reference synchroniser SM2002 is normally fitted. The SM2001 must be known to be serviceable as checked-out in sub-section 4, Section 5, Maintenance in the SM2001 Manual.

(b) Oscilloscope (S.E.Labs SM113 or similar)

(c) Sinewave Signal Source, with outputs from 1.99 mHz to 400 Hz at 2V p-p

8.2 Input Amplifier and Balance Control Board J (SKT J)

S.E.L.Board No.E31495
S.E.L.Assy No.B31497

(a) Connect a link from the junction of R14,R12 and C7 to $0V_e$ on board J.

(b) Connect a known signal source to the EXT SYNC INPUT and the chassis terminal on the rear panel of the SM2001.

(c) With the test oscilloscope, monitor pin 7 of IC18 on board J. Reduce the input voltage gradually and at the same time adjust potentiometer RV1, keeping the displayed squarewave symmetrical. Continue reducing the input voltage until adjustment of RV1 can ho longer maintain the squarewave symmetrical. RV1 should now be at the optimum position.

(d) Disconnect the link, fitted in (a) above.

8.3 1/t Generator Board H (SKT H)

S.E.L.Board No.E31494
S.E.L.Assy No.B31496

(a) Connect a signal source, set to 9.90 Hz at 2V p-p, to the EXT SYNC INPUT terminal and the chassis terminal on the rear panel of the SM2001. Depress the EXT SYNC push-button and check that the push-button lights-up.

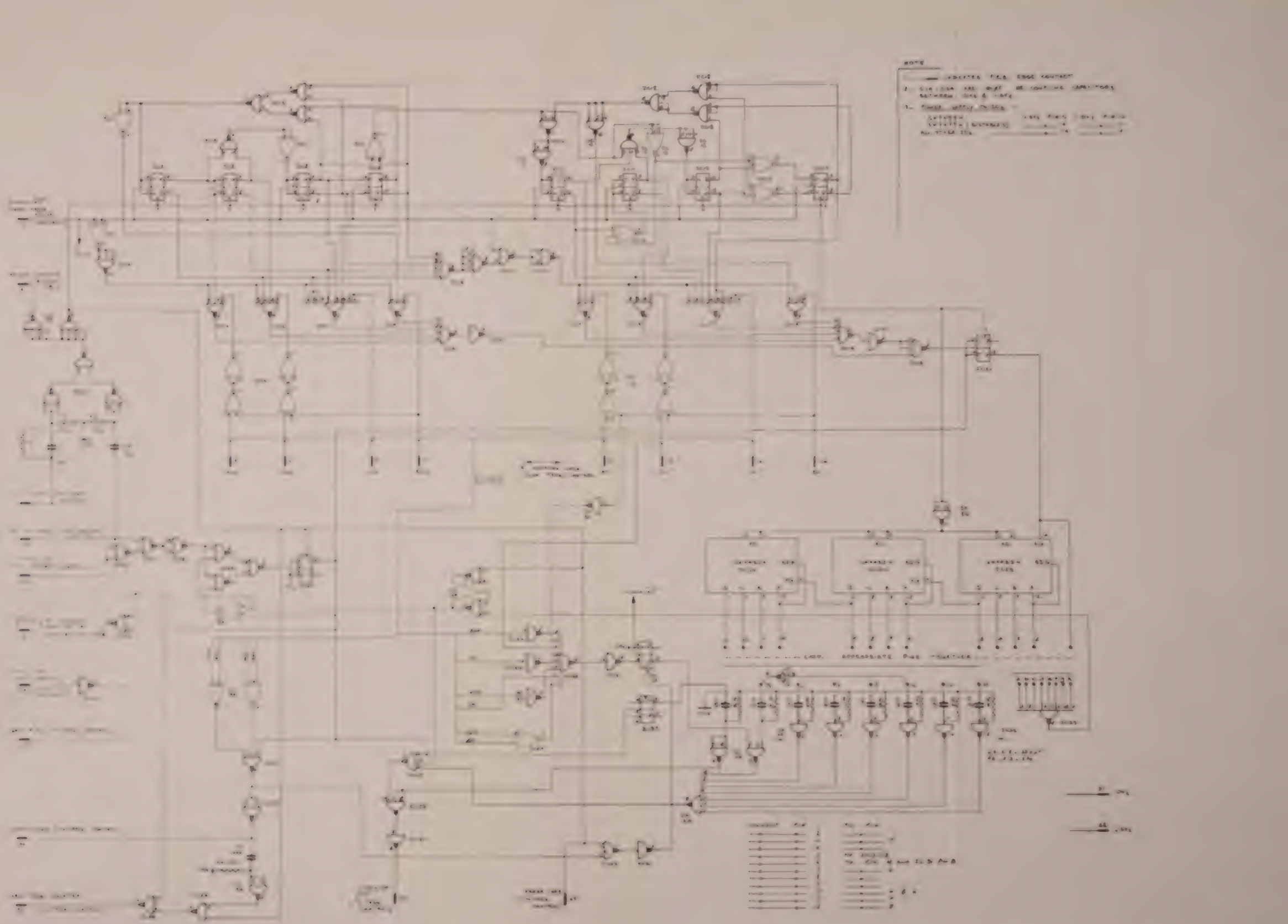
(b) The generator display should now indicate the frequency of the external signal source, to an accuracy of 2%.

(c) Set the frequency of the external signal to 20 Hz (2V p-p) and connect this to the SM2001 CORRELATOR INPUT terminals. The connections to the EXT SYNC INPUT socket should remain. Select 1V ABSOLUTE range on the MEASUREMENT selector.

(d) Select POLAR display and depress the MEASURE push-button. Adjust potentiometer RV2 (on board J) until the centre display indicates a phase shift of less than ±1 degrees.

(e) Set the frequency of the external signal source to the values tabulated below and check that the phase shift is always less than ±1 degrees.

Signal Frequency	Phase Shift (degrees)
400 Hz	< ±1
1.99 Hz	< ±1
199 mHz (milli-Hertz)	< ±1
19.9 mHz	< ±1
1.99 mHz	< ±1



E 32901

TRIGGER O/P (TO I/T GENERATOR) 39

$\overline{I/T}$ (FROM I/T GENERATOR) 3

Ex SYNC I/P 48 (FROM REAR PANEL TERMINALS)

0V 50

R6 1M

D1 D2 2x1N914

$0V_E$

TR1 U267

RV1 1K

R7 22K1

R8 22K1

R14 100K

C7 .10μ

R12 2K74

TR2 BC108

R9 10K

R10 10K

R11 6K19

RV2 1K

R13 15K

R15 6K81

R16 6K81

R19 390

C9 .1μ

TR3 TR4 2x BCY72

R16 1·82K

R18 390

$+17V_E$

C8 .1μ

R20 390

C10 .1μ

D5 17·5, BZY88 C1Z.

IC 1B 710

D3 D4 2x1N914

C11 .1μ

D6 6·8, BZY88, C6V2

R21 680

$-17V_E$

C1 330

R1 270

IC1 IC3

C2 330

R2 270

IC1

$0V_E$ 51

$+5V_E$ 52

$+17V_E$ 54

$-17V_E$ 53

I/T COMMAND 34 (TO I/T GENERATOR)

SYNC. 45 (TO DIGITAL OSC. GENERATOR)

CLOCK $\overline{KF}$ (FROM FREQ. RANGE CONTROL) 13

IC2 SN7493N

IC4 IC9 SN7493N

A/P BD'/P A B C D R0

IC16

IC13 (SN7473N)

C0 330

R5 270

STOP 12 (TO FREQ. RANGE CONTROL)

EXT. 1 (FROM EXT. SYNC. SWITCH)

C3 330

R3 270

IC12

24 QUADRANTS 3 & 4 (SYNC. OUT FROM DIGITAL OSC. GENERATOR)

C4 330

R4 270

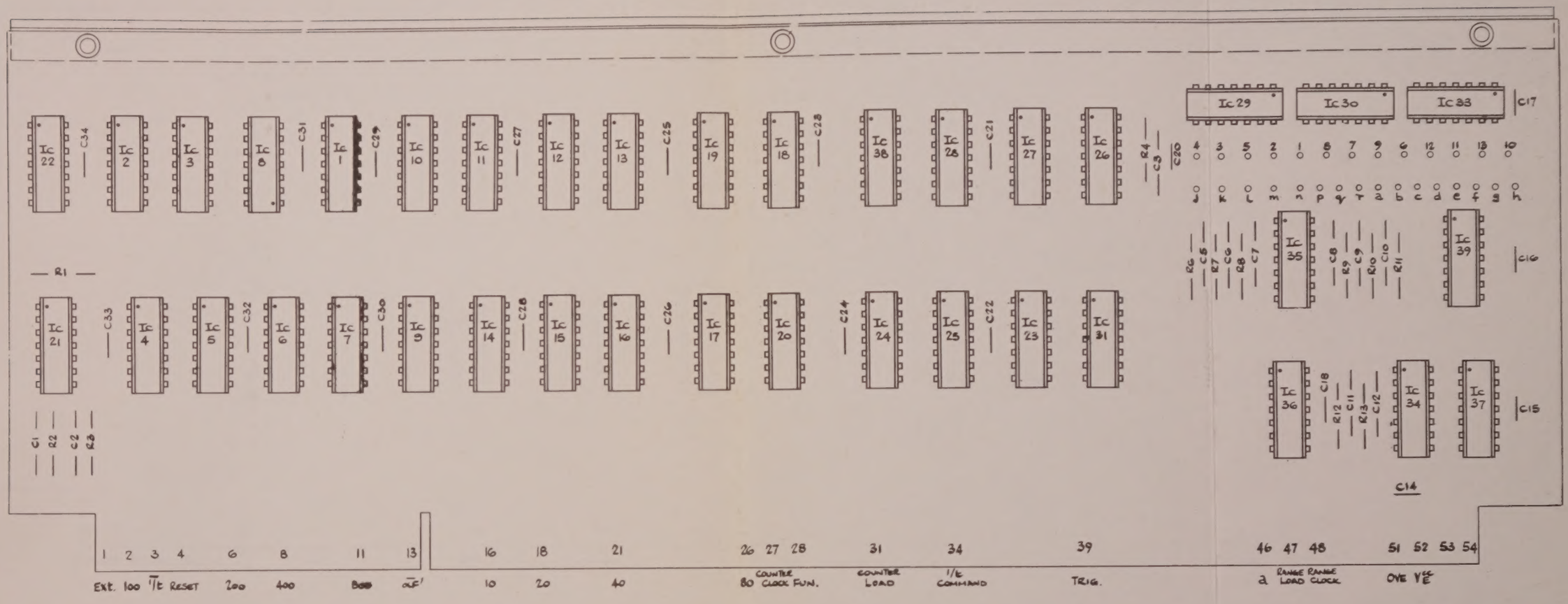
IC5 IC10 IC14 IC17

IC8 IC2

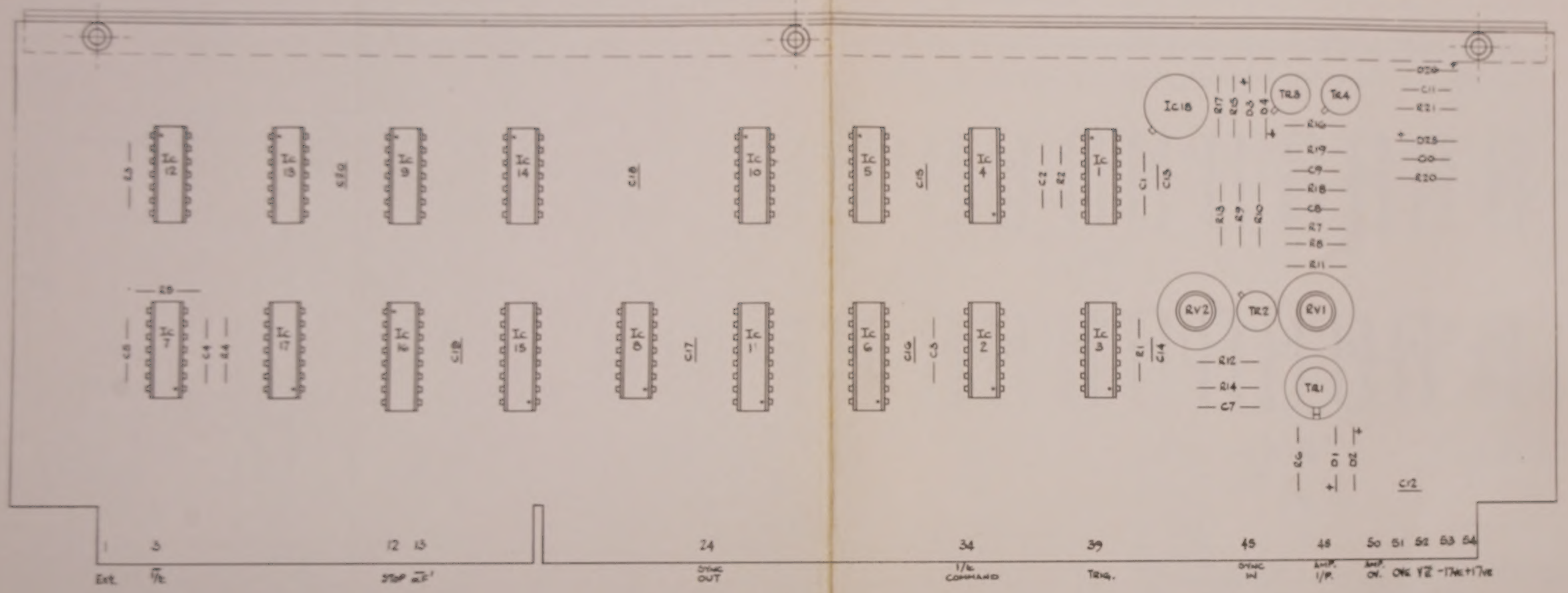
NOTE

1. ——— INDICATES P.C.B. EDGE CONTACT
2. CIR. CKO INCL. (NOT SHOWN) ARE ·01μ DE-COUPLING CAPACITORS BETWEEN $0V_E$ & $+5V_E$
3. POWER SUPPLY TO ICs. :
   SN7493N : $+5V_E$ PIN 5 — $0V_E$ PIN 10
   SN7473N : " PIN 4 — " PIN 11
   ALL OTHER ICs. : " PIN 14 — " PIN 7

TITLE SM200Z BOARD (J) BALANCE CONTROL CIRCUIT DIAGRAM	JIG OR FIXTURE No	PARTS LIST No 3 497	DRAWING No B 32902
	SCALE	SERIES No SM200Z	



TITLE 1/t GENERATOR P.C.B. ASSY.		JIG OR FIXTURE No	PARTS LIST No 31496	DRAWING No B31496
H	SCALE 2:1	SERIES No SM2002		



TITLE: Balance Control - Input Amplifier P.C.B. Assy. J		Parts List No. 31477	Drawing No. B31497
	Scale 2:1	Series No. SM2002	

www.manualsplus.com
1003452

SE LABS (EMI) LTD. North Feltham Trading Estate, Feltham, Middlesex.
Telephone: 01-890-1166 & 5246 (sales); 01-890-5876 (works). Telegrams: Selab, Feltham, Telex: 23995
Northern Sales Office, Bessell Lane, Stapleford, Nottingham. Telephone: Sandiacre 7255

EMI
A member of the EMI Group of companies
International leaders in music, electronics and leisure